THE DESIGN AND PERFORMANCE OF MAGNETIC BUBBLE MEMORY SYSTEMS

by

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A Thesis Presented in Partial Fulfillment
of the Requirements for the Degree
Master of Science in Engineering

ARIZONA STATE UNIVERSITY

May 1984

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ABSTRACT

The advancement of bubble memory technology has progressed tremendously since the concept was initially proposed by Bell Laboratories in 1967. One of the key developments in this area has been the system-level design activity associated with interfacing the bubble memory device to the user's system hardware. This thesis presents the component-level and system-level designs that have resulted in the current architectures of Motorola's 256 kilobit and one megabit bubble memory systems. The individual components of the system are described and evaluated. Various bubble memory system configurations are then presented and system-level trade-offs discussed. The later part of the thesis discusses the overall system performance and compares the bubble memory system performance with that of competitive bubble memory systems as well as other types of storage media.

With all my

Love and Affection

for Helen

"If you have built castles in the air;
your work need not be lost;
that is where they should be;
now put foundations under them."

Thoreau

ACKNOWLEDGEMENTS

I am indebted to many individuals who have expressed inspiration, encouragement and true interest throughout the preparation of this manuscript. I would like to thank Professor George R. Davis, Professor E. Pearse O'Grady, and Professor Ammembal L. Pai for their helpful comments and review of this material. Special thanks are in order for Gerry Walcott who critiqued the original draft and assisted with the recording of some of the performance data. Special thanks are also in order for Jim Stipanuk who alotted the necessary time to pursue this project and who also helped critique the original draft.

Finally, I would like to extend my deepest appreciation to my wife, Helen, who not only typed this manuscript numerous times, but whose patience, understanding and encouragement kept me headed in the right direction.

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CHAPTER 1

INTRODUCTION TO BUBBLE MEMORY TECHNOLOGY

This chapter serves as an introduction to present day bubble memory technology. Its purpose is to acquaint the reader with the basic electromagnetic pheonmena involved with bubble memory devices and will also serve as a necessary aid in understanding the material that follows concerning the designs of each of the peripheral integrated circuits and the overall system architecture.

1.1 WHAT IS A BUBBLE MEMORY?

A Magnetic Bubble Memory (MBM) is a non-volatile solid-state memory device in which information can be stored by forming small cylindrical magnetic domains, called bubbles, whose magnetization is oriented opposite to that of the thin film material in which they exist. Bubbles are termed as such because, by virtue of the Faraday effect, they appear as circular domains when viewed end-on with polarized light under a powerful microscope.

The thin film material is generally an amorphous magnetic-metal film or a single crystal thin film of synthetic ferrite or garnet. This magnetic film exhibits a uniaxial magnetic anisotropy which prevents magnetization in the plane of the film.

Under conditions of no applied external magnetic field, domain structures in the shape of wavy strips form in the magnetic film material with alternating directions of magnetization directed perpendicular to the surface of the film. See Figure 1.1.

When a small applied external magnetic field, called a bias field and denoted H_B, is applied perpendicular to the surface of the film, those domains magnetized in the same direction as the applied bias field increase in volume at the expense of the domains magnetized in the direction opposite that of the applied bias. Thus, the film experiences a process of energy minimization in which it seeks a state of zero net magnetization.

As the applied bias is increased to a certain optimum value, those domains whose magnetic orientation is directed opposite that of the applied bias contract into small cylindrical domains. These small cylindrical domains are typically one to four microns in diameter for present-day technology. Magnetic domains in this state are said to be stable.

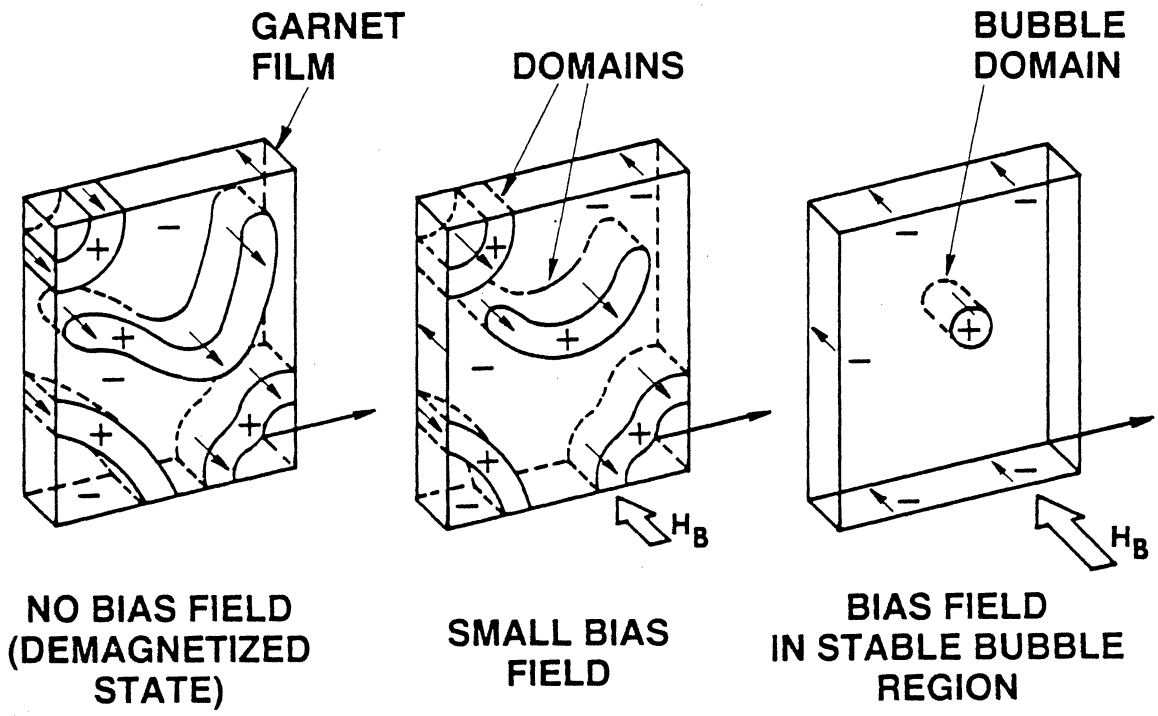


FIGURE 1.1

BASIC BUBBLE MECHANISM

Further increases in the applied bias result in further reductions in the domain size until a critical point is reached, whereby the cylindrical domains collapse, leaving the film magnetically saturated with an orientation similar to that of the applied bias. This condition is known as bubble collapse, and this critical bias field value is called the bubble collapse field.

On the other hand, an applied bias of insufficient strength results in the bubble domain transforming from cylindrical to a long wavy strip. This condition is known as bubble stripout and this critical bias field value is referred to as the bubble stripout field. Therefore, there is a finite range of applied bias, H_B, in which the existence of stable bubble domains is made possible. This region is shown graphically in Figure 1.2 and indicates that the bubble diameter can increase or decrease approximately 50 percent of the mean diameter without experiencing collapse or stripout.

The applied external bias is required for bubble stability and the optimum range for the existence of these small cylindrical domains is approximately 100 to 200 oersteds. Static magnetic fields of this magnitude can be provided by permanent magnets, thereby making the existence of a stable bubble region possible without the need for an external power source. Thus, the use of permanent magnets

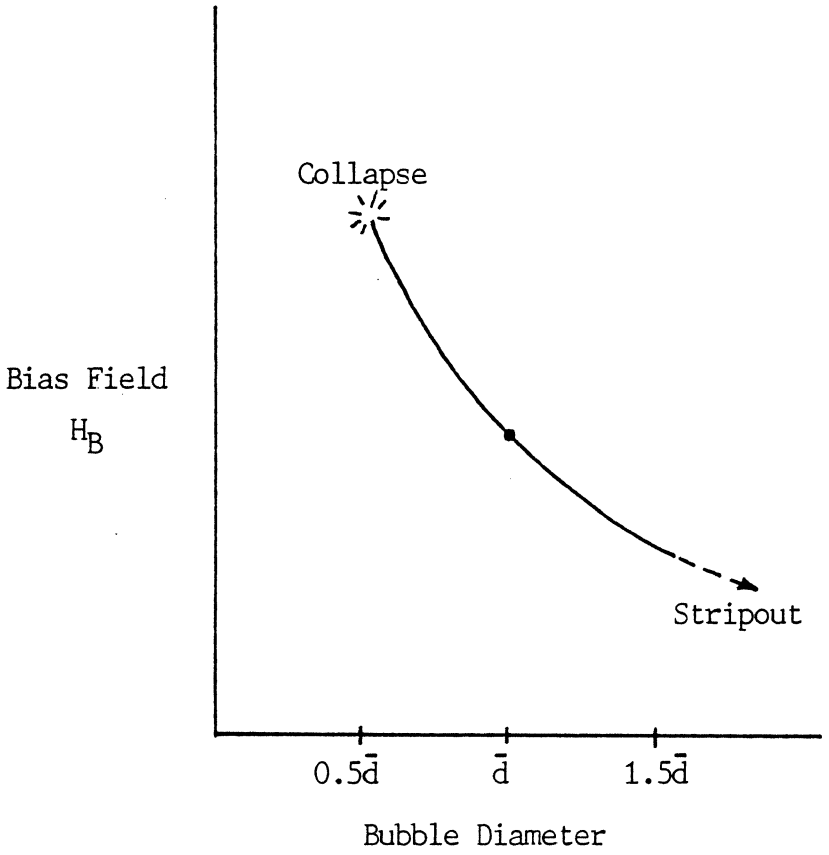


FIGURE 1.2

STABLE BUBBLE REGION

of appropriate strength placed in such a manner that their resultant magnetic field is aligned perpendicular with the magnetic film surface gives the device potential as a non-volatile storage medium.

Logic states are therefore determined by the actual presence or absence of a bubble domain at a particular location within the memory. Typically, the presence of a bubble denotes a logic '1' state and the absence of a bubble denotes a logic '0' state, although the opposite could be equally utilized, depending upon the system designer's preference. For the designs presented in this manuscript, the presence of a bubble denotes a logic '1' state, while the absence of a bubble denotes a logic '0' state.

1.2 BUBBLE PROPAGATION

In the presence of a magnetic field gradient applied parallel to the surface of the thin film, the bubble domains become mobile and are able to move about freely within the thin film in which they exist. Their movements can, however, be controlled when specially shaped structures of magnetically soft nickel-iron (also commonly referred to as permalloy) are deposited upon the surface of the film. These specially shaped structures are known as memory cell geometries and fall into three general categories: the T-bar, the asymmetric chevron, and contiguous disk. See

Table 1.1. Certainly, other memory cell geometries are in use today, but are more or less minor variations of one of the three described here.

In general, bubbles are not allowed to come within four bubble diameters of each other in order to avoid any major interactions among their own local magnetic fields. Thus, the memory cell period of a particular memory cell is dependent upon its particular geometry, current device processing limitations and the bubble domain size (determined by the magnetic film characteristics and subsequently, the applied bias field). Naturally, as the memory cell period becomes smaller, the die storage capacity increases by approximately the square of the reduction in the cell.

The earlier bubble memory devices utilized the T-bar geometry. However, this particular geometry was unacceptable for devices emerging with larger memory capacities, mainly because of the large memory cell period. Most present-day devices employ the asymmetric chevron geometry with memory capacities exceeding four million bits. Future devices utilizing the contiguous disk geometry are expected to have memory capacities of four million to sixteen million bits.

Bubble propagation is therefore accomplished when an in-plane rotating magnetic field, termed a drive field and denoted H_D, is applied across the thin film medium. The

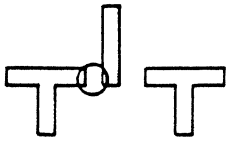
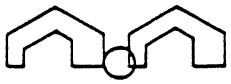
TYPE	GEOMETRY	DIAMETER BUBBLE/MINIMUM FEATURE RATIO	MINIMUM BUBBLE DIAMETER — μ	MEMORY CELL PERIOD μ
T BAR		4/1	5	24
ASYMMETRIC CHEVRON		1.5/1	2	8
CONTIGUOUS DISK		1/1	1	4

TABLE 1.1

BASIC MEMORY CELL GEOMETRIES

rotating magnetic field induces magnetic polarities within the permalloy geometries deposited atop the magnetic film. The induced magnetic polarities vary according to the present direction of the applied rotating magnetic field. The bubble domains tend to follow the polarization of the permalloy geometries and thereby propagate from one memory cell to another, moving one memory cell every rotation of the drive field.

Figure 1.3 illustrates bubble propagation in a serial string of chevron-shaped memory cells which are deposited on a magnetic film. Assume the bias field is at an optimum value such that stable, cylindrical bubble domains exist. The chevron patterns, being magnetically soft, become magnetized when in the presence of a magnetic field rotating in the same plane. The asymmetric geometry of the chevron results in changes in the polarity of its magnetization such that a bubble effectively sweeps beneath the entire chevron in one full rotation of the in-plane rotating magnetic field. Propagation in the T-bar and contiguous disk geometries is accomplished in a similar manner.

Drive field frequencies of from 50 to 150 KHz are typical in today's bubble memory devices. Drive field magnitudes are generally on the order of 40 to 80 oersteds.

Clearly, one possible implementation of the bubble memory concept is a shift register of considerable length.

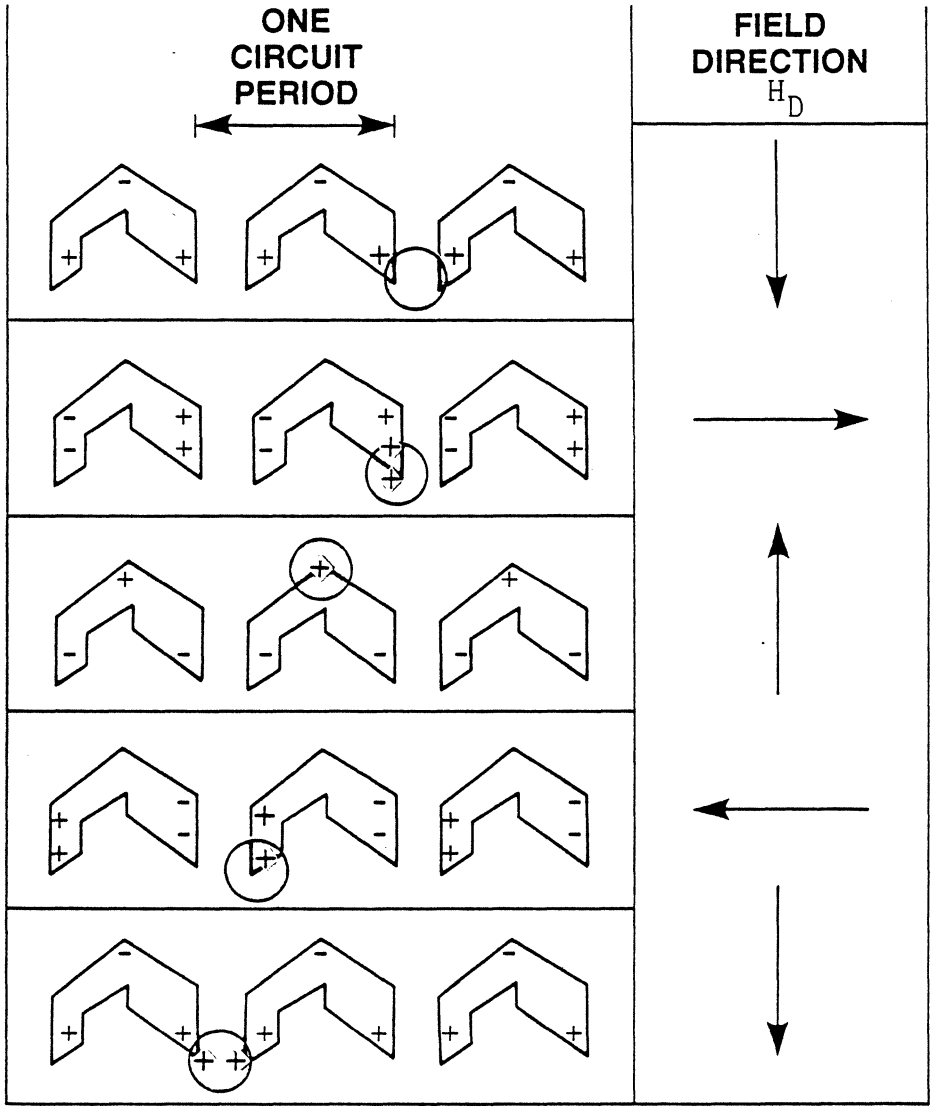


FIGURE 1.3

BUBBLE PROPAGATION UNDER PERMALLOY CHEVRONS

In this case, bubbles shift one memory cell period every single rotation of the drive field. Later, it is shown that this concept is indeed implemented in the architectures of large capacity bubble memory devices.

1.3 BUBBLE DETECTION

The detection of magnetic bubble domains is quite simple in theory, but unfortunately, in actual applications the technique becomes somewhat more complex. Detection of magnetic bubble domains makes use of the magnetoresistance effect of a permalloy element called a detector.

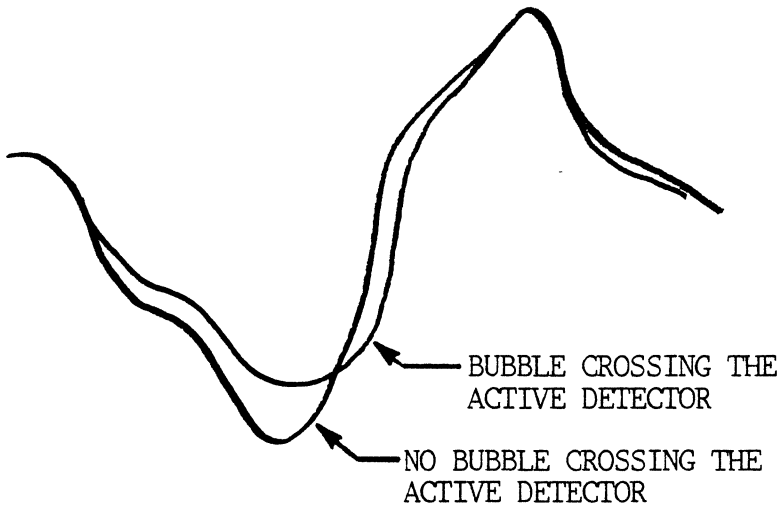
When a direct current is passed through a permalloy detector which is in the presence of a magnetic field whose orientation is perpendicular to that of the current direction, the resistivity of the permalloy will undergo a minute change. Resistance changes in the detector are also induced by the presence of the in-plane rotating drive field, H_D. For this reason, a reference, or dummy, detector is provided in the same general location so that the effects of resistance changes due to the rotating drive field appear as common mode signals and can be effectively cancelled out when a differential amplification of the resulting voltage signals is performed.

The transmission of a bubble domain beneath the so-called "active detector element" creates a small increase

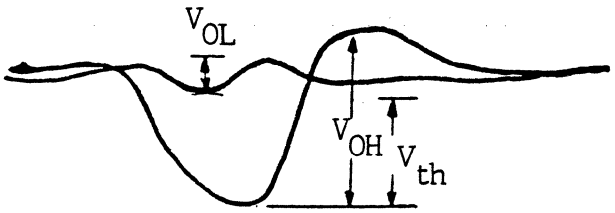
in the resistance of that detector element and a corresponding change in the voltage dropped across the element, provided a constant current is sourced through it. In most bubble memory devices the bubble domains are prevented from crossing beneath the reference detector by a guard rail which annihilates the bubble domain after it has crossed beneath the active detector. Now a differential amplification of the active and reference detector voltages will result in a voltage waveform proportional to the change in resistance of the active detector when a bubble domain crosses beneath it. Provided that it were possible to perfectly cancel the effects of the rotating drive field, the differential voltage would be identically zero when no bubble domains were present.

Typical common mode and differential output voltage signals for both a bubble crossing the detector and no bubble crossing the detector are superimposed in the illustrations of Figure 1.4.

In order that sufficient magnetic flux is produced by a single bubble domain crossing the active detector element to significantly alter the active detector resistance, the bubble domain (if one was present) is stretched out to a length of several hundred times the original diameter before it enters the detector region. This stretching process is



(a) AC COMMON MODE DETECTOR SIGNALS



(b) DIFFERENTIAL MODE DETECTOR SIGNALS

FIGURE 1.4

BUBBLE MEMORY DETECTOR SIGNALS

achieved within a matter of a few periods of closely spaced chevron stacks physically located adjacent to the active detector. This concept is illustrated in Figure 1.5.

It should be noted that the peak-to-peak amplitude of both the '1' and '0' signals (V_{OH} and V_{OL}, respectively) are not only dependent upon detector current, permalloy concentration, drive field and bias field but also upon the local magnetic fields of bubble domains located adjacent to the detector element. Since detection is performed in a serial manner, this makes the output signal amplitudes sensitive to particular data patterns. However, provided that the bubble-to-zero signal margin (i.e., signal-to-noise) is sufficiently large and the detector threshold trip point, V_{th} is properly set, these minor variations in detector output signal amplitude will not in any way affect detection reliability. It should be noted that as the bubble memory temperature increases, the detector output signal decreases in amplitude.

1.4 THE NON-DESTRUCTIVE READ OPERATION

Consider a long string of chevron structures (like that shown in Table 1.1) deposited atop a thin magnetic film and arranged in a loop such that it forms a long circular shift register. Recall that data (the physical presence or absence of bubble domains) in this long shift register is

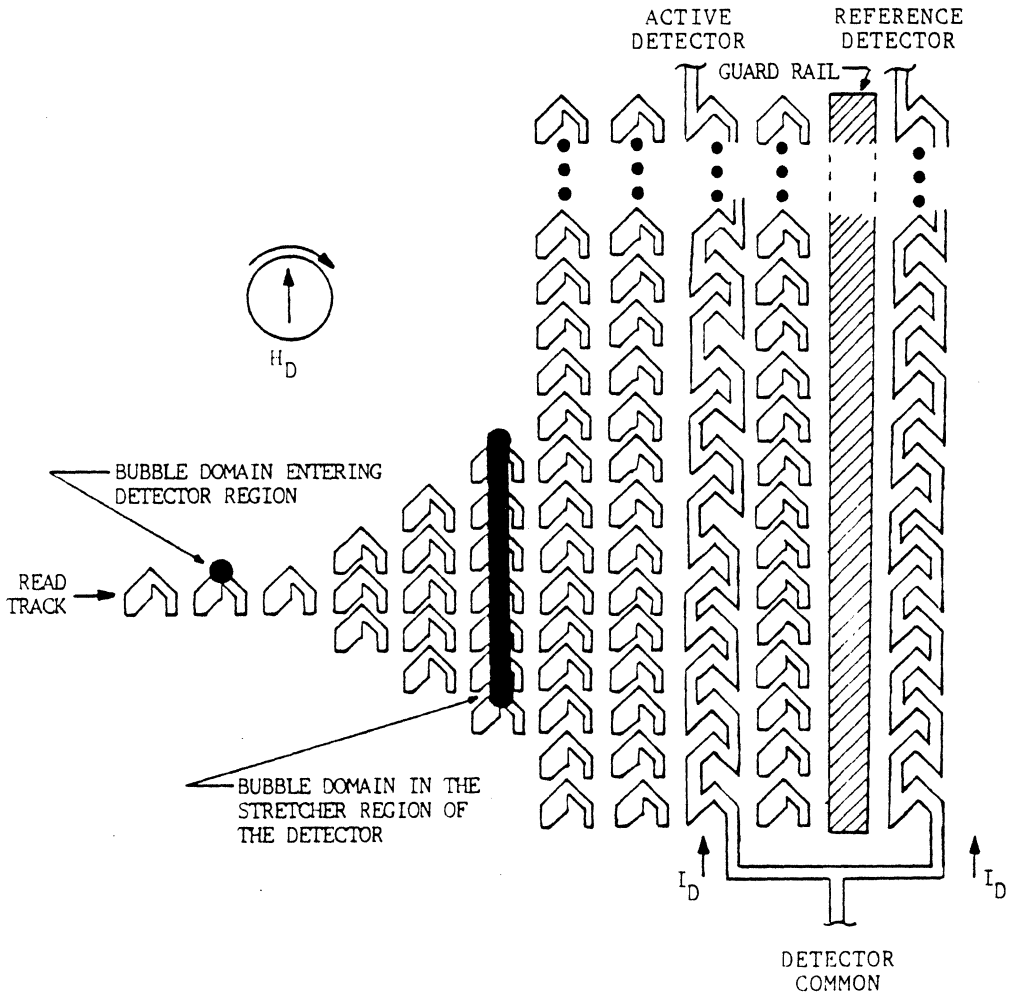


FIGURE 1.5

BUBBLE MEMORY DETECTOR REGION

simultaneously and serially circulated around the loop when influenced by an in-plane rotating magnetic drive field, H_D. Recall also that the bubble domains are restricted to small cylindrical shapes by a static magnetic field of appropriate intensity and oriented orthogonal to the plane of the thin film.

Some means must now be provided to non-destructively read a data bit from the loop and, provided the data bit is a bubble domain (i.e., logic '1'), propagate a bubble domain to the detector element so it can be sensed by external circuitry. The path of chevron structures by which bubble information leaves this loop and propagates to the detector elements is known as the output or read track. If the data bit is not a bubble domain (i.e., logic '0'), then nothing is propagated to the detector.

The process of non-destructively reading bubble data is known as replication. The means by which this is accomplished is to apply a bi-level current pulse to a gate element known as the replicate gate. Obviously, some means must be provided to keep track of the whereabouts of data with respect to the replicator at any particular instant of time, however, for now it suffices to say that this matter is being handled externally and the replicate current pulse is applied at the proper time. See Figure 1.6.

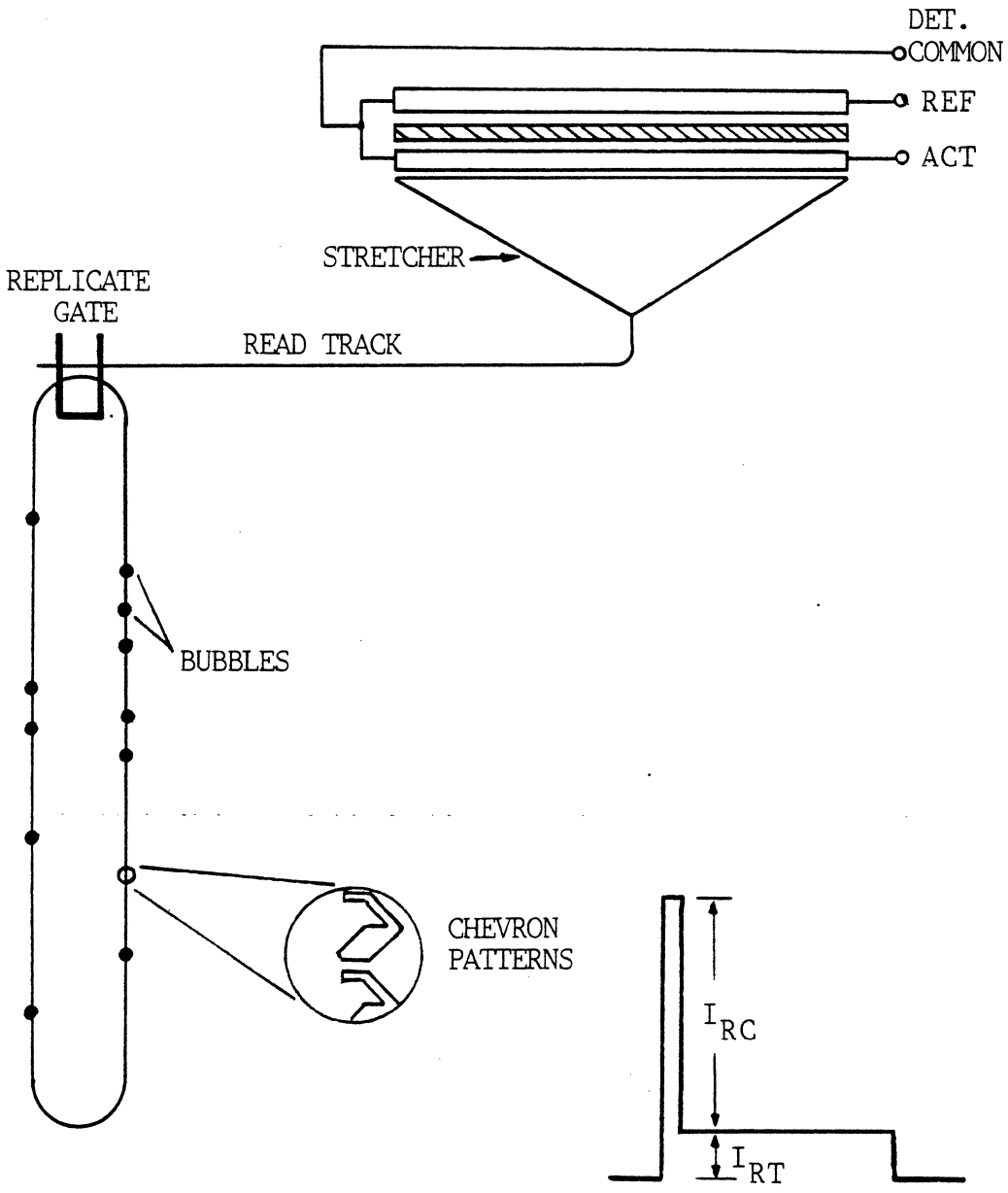


FIGURE 1.6

BUBBLE MEMORY READ OPERATION

As a bubble domain propagates under the replicate gate located at one end of the loop, it is stretched into a strip as it turns the corner of the loop. A narrow, relatively high-level current pulse applied to the replicate gate at this time establishes a very localized magnetic field which acts to split the domain in two. This high-level current pulse, I_{RC}, is referred to as the cut pulse. The interaction of the local magnetic fields of the two resulting domains prevents them from recombining. A wider and lower current pulse, known as the transfer-out current, I_{RT}, applied to the replicate gate immediately following the cut pulse serves to transfer the trailing bubble domain out onto the read track, while the other domain remains in the storage loop. The domain on the read track can then be propagated to the detector element to be sensed by external circuitry. A replicate gate performing this replication process is illustrated in Figure 1.7. Thus, this process of "cloning" bubbles and detecting replicas of the original data performs a non-destructive read operation.

1.5 THE WRITE OPERATION

Consider again the circular shift register made up of permalloy chevrons deposited on top of a magnetic film as discussed in Section 1.4. The memory write operation is functionally a two-step process in which a bubble domain must first be created (provided a logic '1' is to be stored

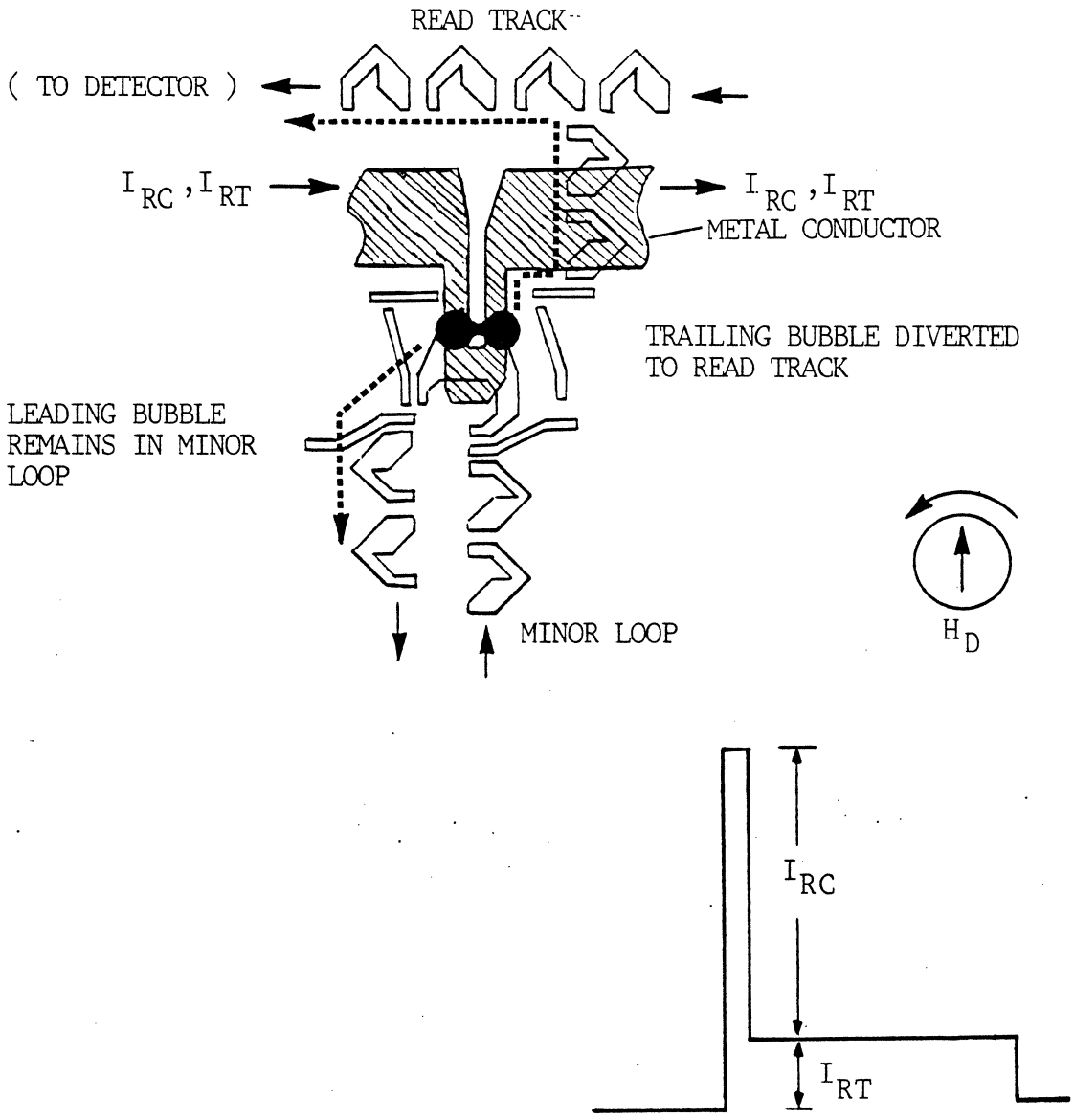


FIGURE 1.7

BUBBLE REPLICATION PROCESS

in the loop) and then somehow exchanged with the old, existing data presently contained in the loop.

Creation of bubble domains is accomplished by a process of nucleation from a gate element known as a generator. (Some bubble memory devices, however, use a replicator-type element with a small separate loop and replicate a "seed" bubble, rather than nucleate bubble domains.) A high-level current, I_G, of sufficient magnitude is momentarily applied to the generator to produce a localized magnetic field directed opposite to the static bias field and film magnetization in the region of the generator "hairpin". This creates a localized inversion in the film magnetization, resulting in the creation of a single bubble domain. This bubble domain can then be propagated to the loop for storage. A generate gate is illustrated in Figure 1.8. Care must be exercised in not allowing the current to fall too sharply on the trailing edge of the pulse, however, since this condition may result in the spontaneous nucleation of additional unwanted bubble domains.

Assuming a logic '1', once the bubble is nucleated, it must be propagated to the storage loop. The path of chevron structures by which bubble information propagates from the generator to the storage loop is known as the input or write track. See Figure 1.9.

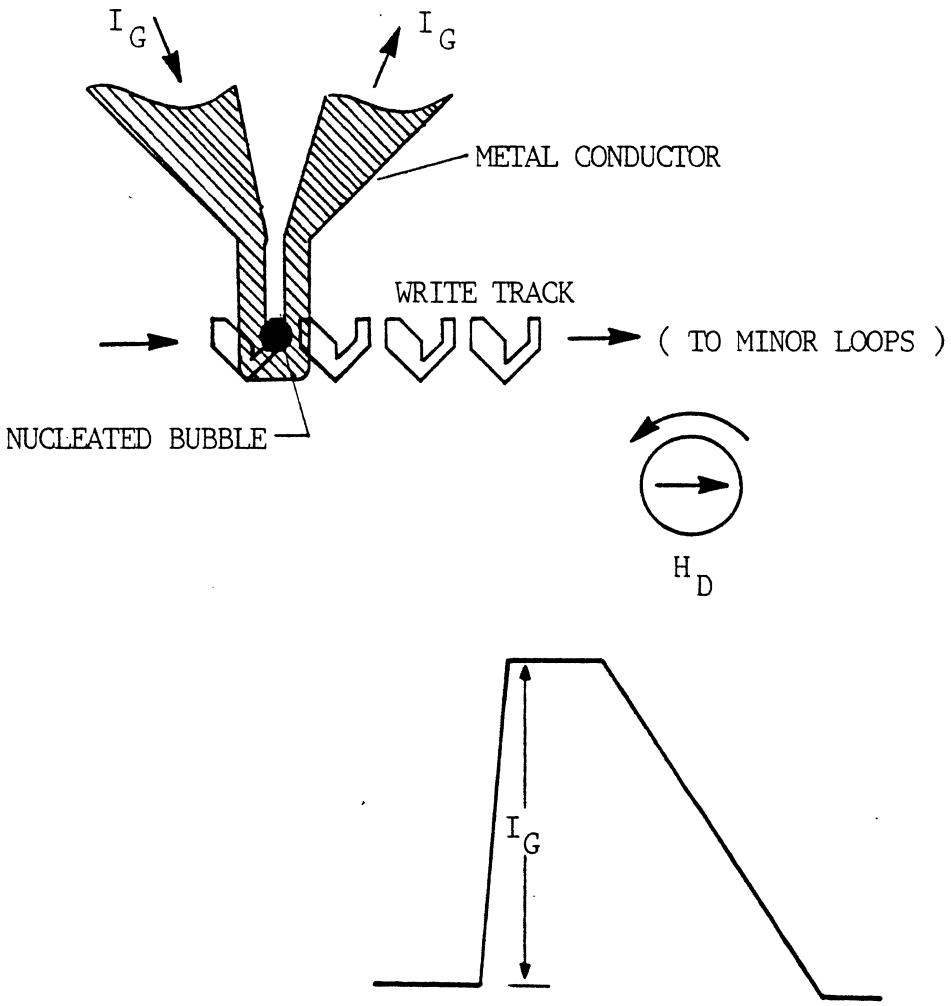


FIGURE 1.8

BUBBLE NUCLEATION PROCESS

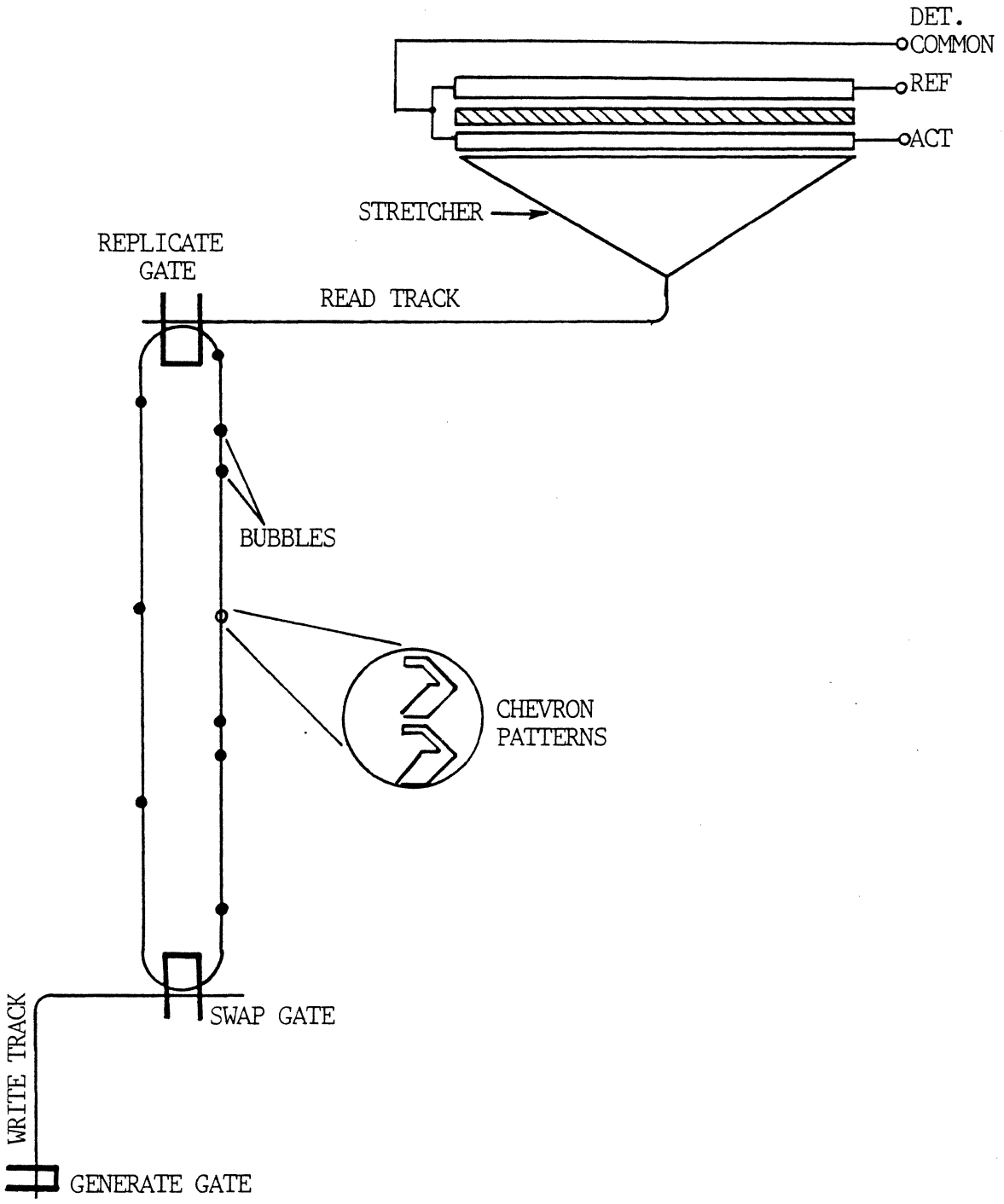


FIGURE 1.9

BUBBLE MEMORY WRITE OPERATION

At the time when the bubble domain reaches one end of the loop, the old data bit presently stored in the loop is aligned adjacent to it and both are under a gate element known as the swap gate. (Once again, assume the timing for this alignment of data has been provided for externally.) Now, a low-current pulse applied to the swap gate for nearly one full rotation of the drive field, H_D, causes the old data bit to be diverted and transferred out onto the write track, while the new data bit is simultaneously transferred into the storage loop. The old data bit can then be propagated off the end of write track and annihilated, thus completing the memory write cycle. Figure 1.10 illustrates the swap gate operation.

Earlier bubble memory devices did not use the swap architecture discussed above. Rather, they used a transfer-in gate (unidirectional transmission) to store data in the loop. This was preceded by applying only the transfer-out current to the replicate gate which was located on the opposite end of the loop. This action clears the data bit in the corresponding memory location of the serial data loop. The empty memory location could then be propagated down to the transfer-in gate for writing of new data. Obviously, the swap architecture has the distinct advantage of reducing the average memory write cycle time by approximately one-half, since propagation to the replicator first is unnecessary.

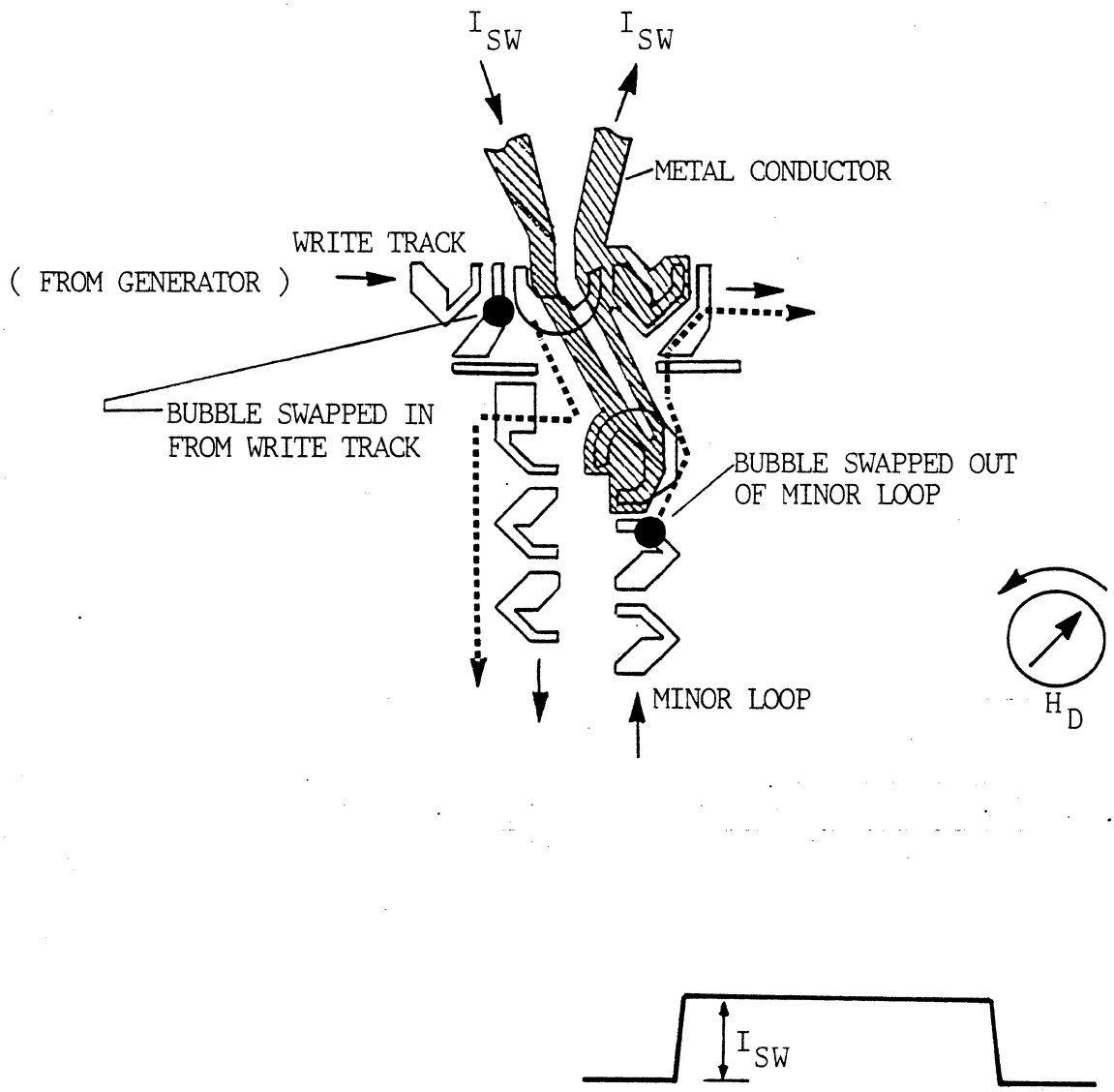
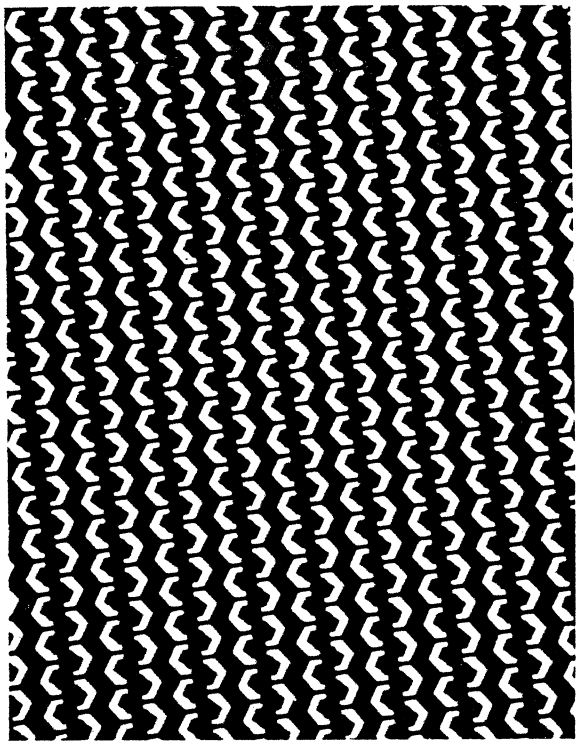


FIGURE 1.10

BUBBLE MEMORY SWAP PROCESS



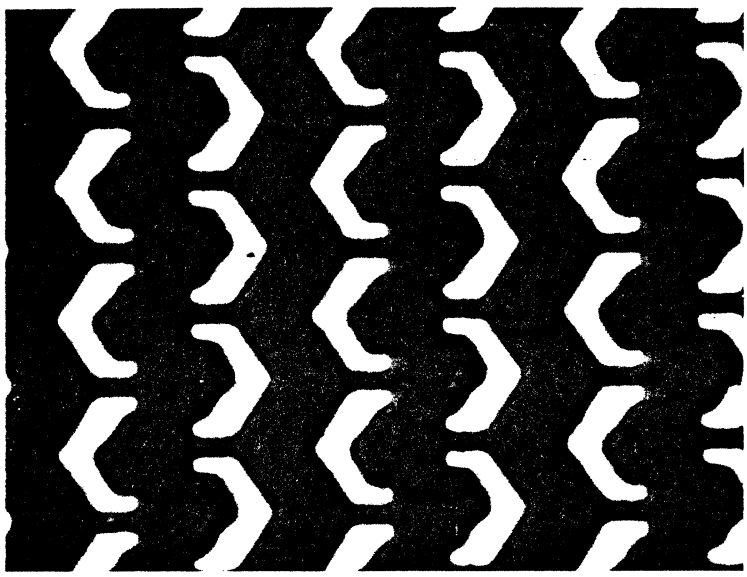


FIGURE 1.11

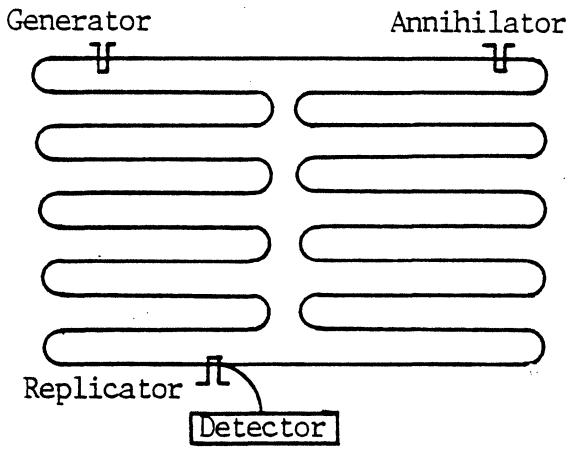
BUBBLE MEMORY STORAGE CELLS

A photograph of an actual bubble memory storage area is shown in Figure 1.11.

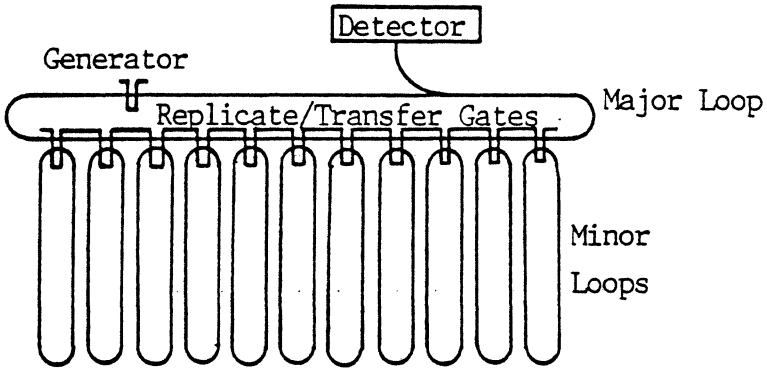
1.6 BUBBLE MEMORY DEVICE ARCHITECTURES

Several types of architectures are used in the design of bubble memory devices. Basically, all the architectures are iterations of the shift register loop example used throughout sections 1.4 and 1.5. The device organizations can be classified into the following three categories: (a) serial loop architectures, (b) major/minor loop architecture and (c) block swap/replicate architecture. These are illustrated in Figure 1.12.

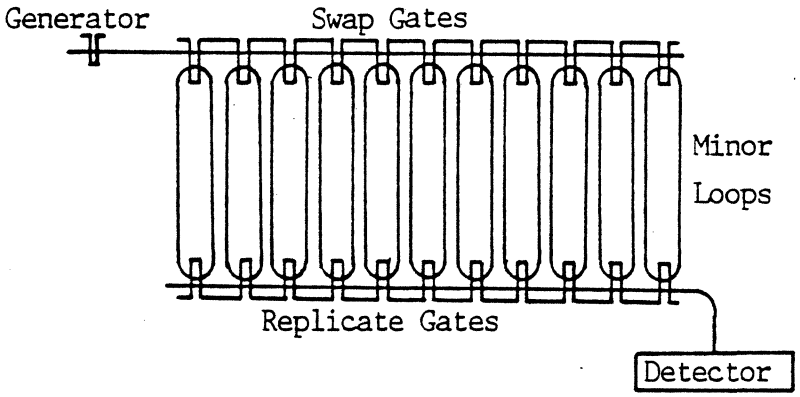
The serial loop architecture consists of a single very long storage loop. A generate gate, an annihilate gate and a replicate gate are provided for writing and reading of data. This architecture has a major disadvantage in that a single processing defect in the loop will result in the entire memory being inoperative. Access times are also usually quite lengthy, with the average read access being equal to one-half the loop length plus the length of the read track from the replicator to the detector. As an example, a one megabit serial loop bubble memory device operating at 100 KHz drive field frequency will have an average read access time of greater than five seconds!



(a) Serial Loop Architecture



(b) Major/Minor Loop Architecture



(c) Block Swap/Replicate Architecture

FIGURE 1.12

BASIC BUBBLE MEMORY ARCHITECTURES

Significant reductions in access time for the same memory capacity can be obtained by using the major/minor loop or block swap/replicate architectures. In these device architectures, data are written to and read from many minor loops in parallel, thus reducing the average read access time to one-half the minor loop length plus the length of the read track from the nearest replicate gate to the detector. Since the length of the minor loops are several orders of magnitude shorter than a serial loop architecture device with the same memory capacity, approximately several orders of magnitude in reduced access time can be obtained. A one megabit bubble memory of this type with 512 minor data loops of 2048 bits each operating at 100 KHz will therefore have an average read access time of approximately 11 milliseconds.

For these two device architectures, a single generate gate is provided and data are nucleated serially and propagated along the write track (or minor loop). The swap gates (or replicate/transfer gates) of all minor loops are connected in series so that writing into the minor loops by the swap (or transfer-in) pulse supplies new data to all minor loops simultaneously after data are aligned. Likewise, the replicate gates of all minor loops are connected in series so that data are replicated out onto the read track (or major loop) in parallel and serially propagated to the detector.

The block swap/replicate architecture is sometimes organized in a dual arrangement. This basically serves to split up incoming adjacent data bits (via the second generate gate) into odd and even data bits stored on opposite halves of the die. Following a read operation, the odd and even data are interleaved before entering the detector.

The major advantage of the major/minor loop and block swap/replicate architectures is that many additional minor loops than is required for actual data storage can be provided. Thus, processing defects will render only a minor loop inoperative rather than the entire memory, resulting in increased yields. These additional minor loops are known as redundant loops and can be excluded from accepting data during a write operation by inserting zeros in the generate data stream. Likewise, during the read operation external circuitry removes these zeroes from the output data stream and then compresses the remaining data.

Obviously, the external circuitry must be made aware of which bit positions (i.e., which minor loops) are redundant. This is encoded onto the label of the bubble memory device and can be stored in RAM, PROM, or typically in a separate loop within the bubble memory itself. This separate loop is referred to as the map loop (or bootloop) and the information it contains regarding which loops are

redundant is referred to as the redundancy map information (denoted RMPI). The weakest of all minor loops are identified during final test of the device and this information is subsequently encoded and loaded into the map loop.

External circuitry is therefore informed of the RMPI during a system initialization in which the map loop is read, via its own map replicate gate, and temporarily stored externally for future use in formatting the input and output serial data streams.

CHAPTER 2

THE BUBBLE MEMORY DESIGN CHALLENGE

The purpose of this chapter is to outline the strict operational requirements of the magnetic bubble memory device. The chapter then concludes with a breakdown of tasks into several LSI components which have been designed to service the bubble memory.

2.1 REQUIREMENTS OF THE MBM DEVICE

In Chapter 1, it is shown that operation of a bubble memory device is accomplished when certain external stimuli are applied to the composite structure of permalloy, magnetic film, and metal conductor. Among these external stimuli are the rotating magnetic field, H_D, which serves to propagate bubble domains in the storage loops and along the read and write tracks. To supply the MBM with this drive field, two coils are provided as an integral part of the memory device. See Figure 2.1. Termed the X and Y coils, they are physically placed orthogonal to each other around the MBM die and require periodic triangular currents sourced through them at 90 degrees out of phase with each other. This produces a vector sum magnetic field which rotates in the plane of the thin magnetic film. See Figure 2.2 Since

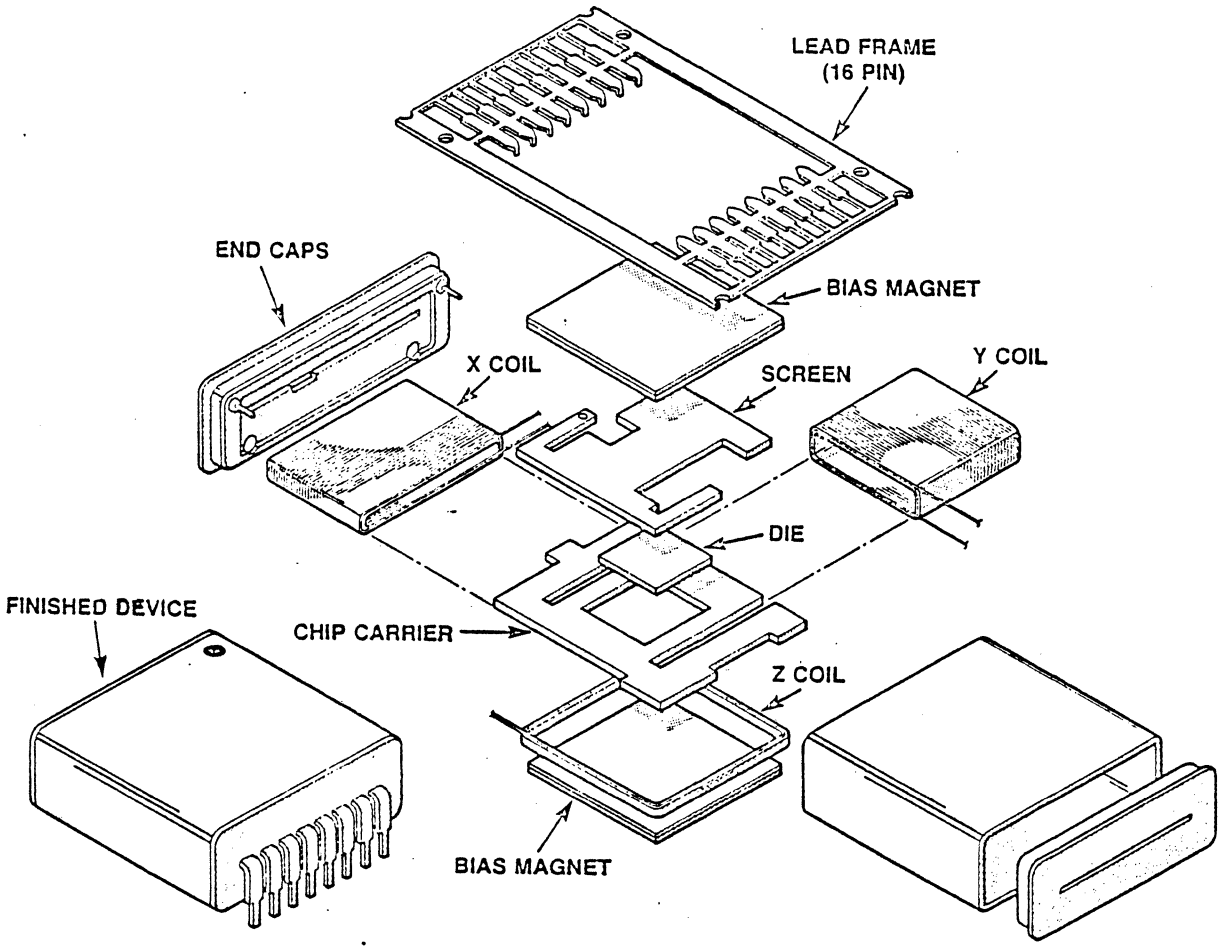
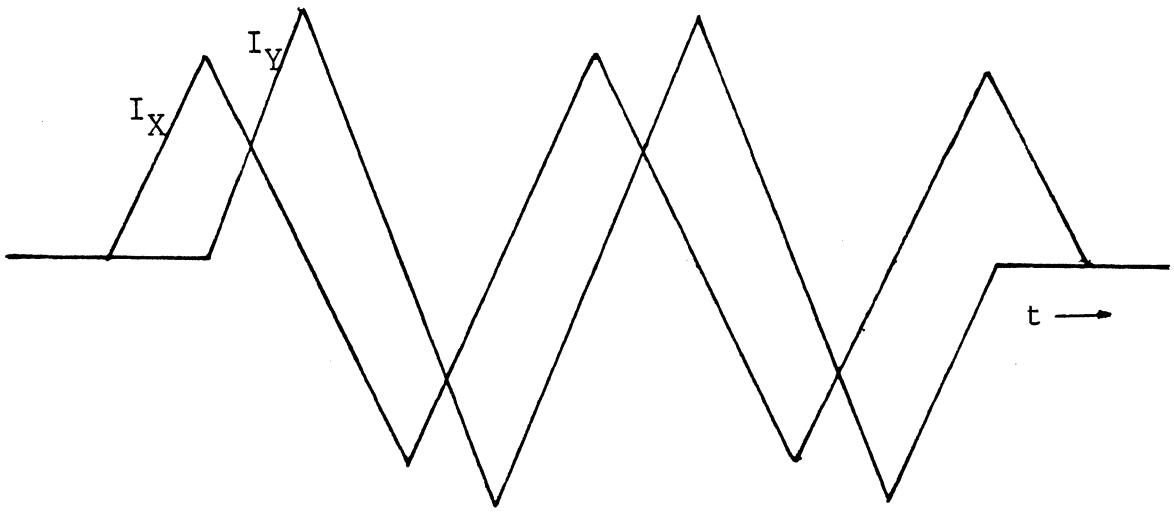
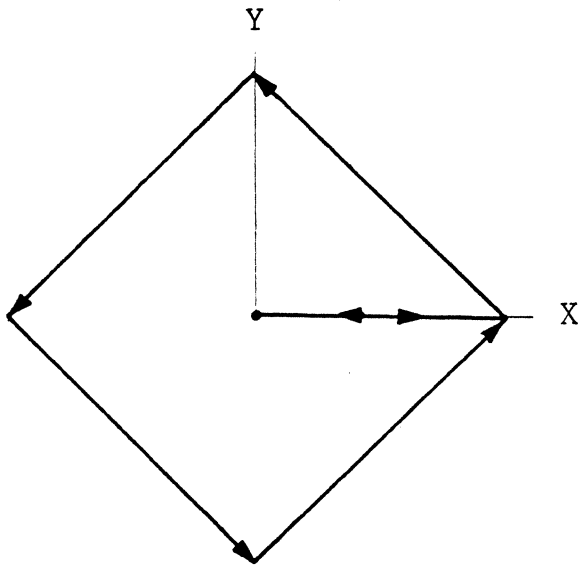


FIGURE 2.1

INTEGRAL PARTS OF A BUBBLE MEMORY



(a) X AND Y COIL DRIVE FIELD CURRENTS



(b) IN-PLANE DRIVE FIELD VECTOR

FIGURE 2.2

BUBBLE MEMORY DRIVE FIELD

one coil (i.e., the Y coil) is physically placed slightly further away from the die when it encapsulates the other coil and die carrier, its peak current amplitude must be greater than that of the closer coil (i.e., the X coil) to produce an equivalent effect. The coil inductances and resistances of the X and Y coils are therefore designed with this characteristic in mind. The actual magnitudes of the coil currents are also very important since a sufficient field must be created to reliably propagate bubble domains beneath the permalloy chevrons and more importantly, across the gaps. Typical X coil currents are approximately 1.3 amperes (peak-to-peak) and typical Y coil currents are approximately 1.5 amperes (peak-to-peak).

A third coil is also provided as an integral part of the bubble memory device. This coil, called the Z coil, is used to completely clear the device. A large dc current (approximately 3 amperes) applied through this coil in such a direction that the resulting magnetic field aids the bias field will result in bubble collapse, thus clearing the memory device of all existing bubble domains.

Through experimentation, it has also been determined that the start-up and shut-down sequencing of the coil currents is crucial to reliable device performance. Incorrect sequencing or overshoot during the shut-down sequence have proved to be detrimental to proper bubble pro-

pagation and subsequently, data non-volatility. Extreme care must be exercised when switching coil currents on and off.

In general, the function currents (i.e., swap, replicate, map replicate, and generate) have very stringent requirements not only in peak amplitude, but also in rise/fall times and phase of the bubble propagation cycle. The replicate-cut current is particularly unforgiving if the time at which it is applied relative to the bubble propagation cycle varies from a known nominal value. That is, the replicate-cut function has a small phase margin and must be tightly controlled. Over temperature, the amplitude of the cut pulse must change from some bubble memory devices, such as Motorola's one megabit MBM2011.

While the generate current has a relatively wide amplitude margin and phase margin, it is necessary that the fall time be slow enough to prevent the production of additional, unwanted bubble domains. These unwanted bubbles have the potential for being accidentally stored in the minor loops, thus producing hard, excess-1 errors.

Since the swap current is a long, low-level current pulse, its phase margin is relatively wide, however, the amplitude must be tightly maintained.

Thus the bubble memory device has an operating region defined by the bias field, drive field, function currents and temperature. This operating region is shown graphically in Figure 2.3.

For reliable detection, constant dc currents matched to within a few percent must be sourced through the active and reference detectors of the bubble memory device. The resistances of the active and reference detector must also be matched to within 1.5 percent. As discussed briefly in Section 1.3, a differential amplification of the resulting active and reference detector voltages will result in a voltage signal proportional to the change of resistance of the active detector under the influence of the bubble domain. However, the differential amplifier must have very good common mode rejection (CMR) to cancel the effect of the drive field, H_D, which has an effect approximately one hundred times that of the bubble domain.

To complicate the situation, the bubble detector sensing scheme must be able to reliably operate in the presence of noise at its supply and ground inputs. Since the X and Y coil currents are simultaneously propagating the bubble domains across the active detector, they act to significantly increase induced noise on the supply and ground.

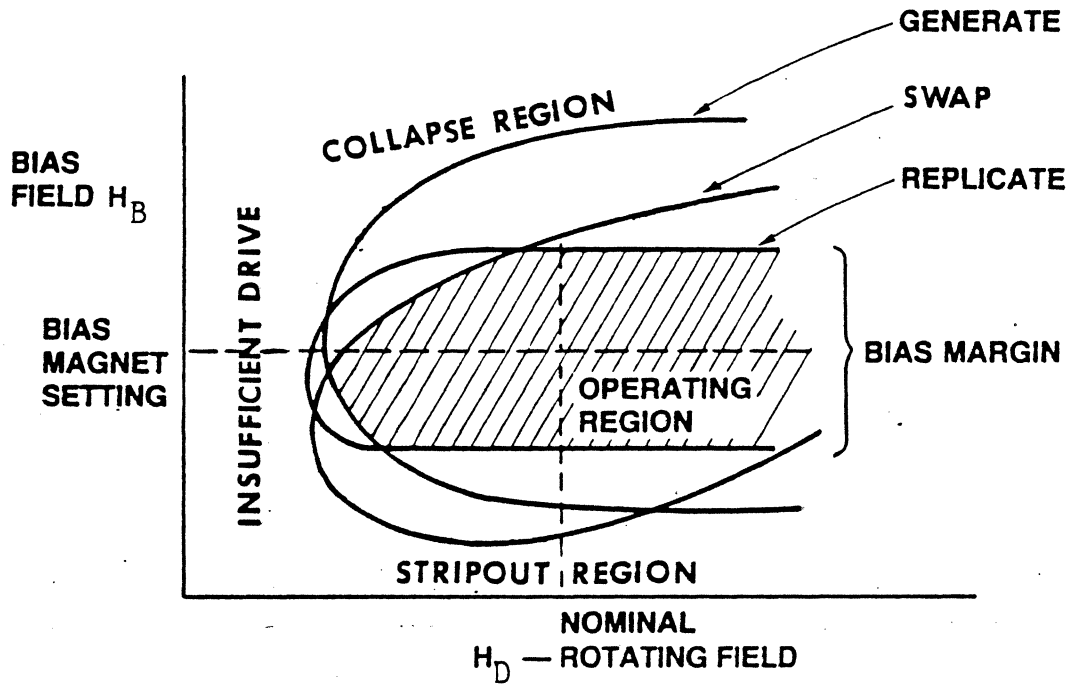


FIGURE 2.3

BUBBLE MEMORY OPERATING REGION

A means of monitoring all the system timing must be provided. Timing for the drive field (including orderly start-up and shut-down), the function currents, and gating for the sensing operation must be tightly controlled. Output and input formatting of the data streams by deleting and inserting zeroes, respectively, into those positions corresponding to redundant loops must also be handled.

To improve overall system reliability, it is advantageous to include error detection and correction capability in the system design. It is best if this function can be provided so that it takes place in a transparent manner, thereby requiring minimal user intervention.

Finally, the entire system which performs the operations stated above should be able to easily interface to popular microprocessor interface bus structures. But at the same time, the programmability of the entire MBM system should be kept as simple as possible.

2.2 ALLOCATION OF TASKS

Now that the requirements of the bubble memory device have been defined, the overall system architecture can be developed. The system development process described here is that which resulted in the present architectures of Motorola's 256 kilobit and one megabit bubble memory systems.

The system functions are logically composed of four basic operations; that is, (a) providing a means of sensing bubble data, (b) providing the drive field to propagate bubbles, (c) providing the function currents to nucleate, replicate, and swap bubbles, and (d) controlling all the system timing including redundancy formatting, error detection and correction and address management.

A bubble memory sense amplifier integrated circuit provides the capability of sensing bubble domains crossing the active detector element. It converts this low-level voltage output of the bubble device into a serial digital data stream corresponding to the information crossing the MBM active detector element.

A bubble memory coil predriver and driver circuit provide the necessary voltage swings to the MBM X and Y coils to source the out-of-phase triangular current waveforms that result in a magnetic drive field of sufficient magnitude to reliably propagate bubble domains within the device.

A bubble memory operation current driver provides all the specialized function currents, including controlled rise and fall times, to the MBM device that are required during the processes of reading and writing bubble data.

Finally, a bubble memory controller manages all system timing for the coil predriver and drivers, sense amplifier, and operation current driver. In addition, it handles all redundancy formatting automatically and transparently and is designed to easily interface to most microprocessor bus structures. Automatic error detection and correction is an added feature that works to improve overall system reliability.

Figure 2.4 is a functional block diagram detailing a one-device bubble memory system and its interface to a microprocessor bus structure.

The design of two bubble memories and each of the peripheral integrated circuits which service them are discussed in more detail in Chapter 3.

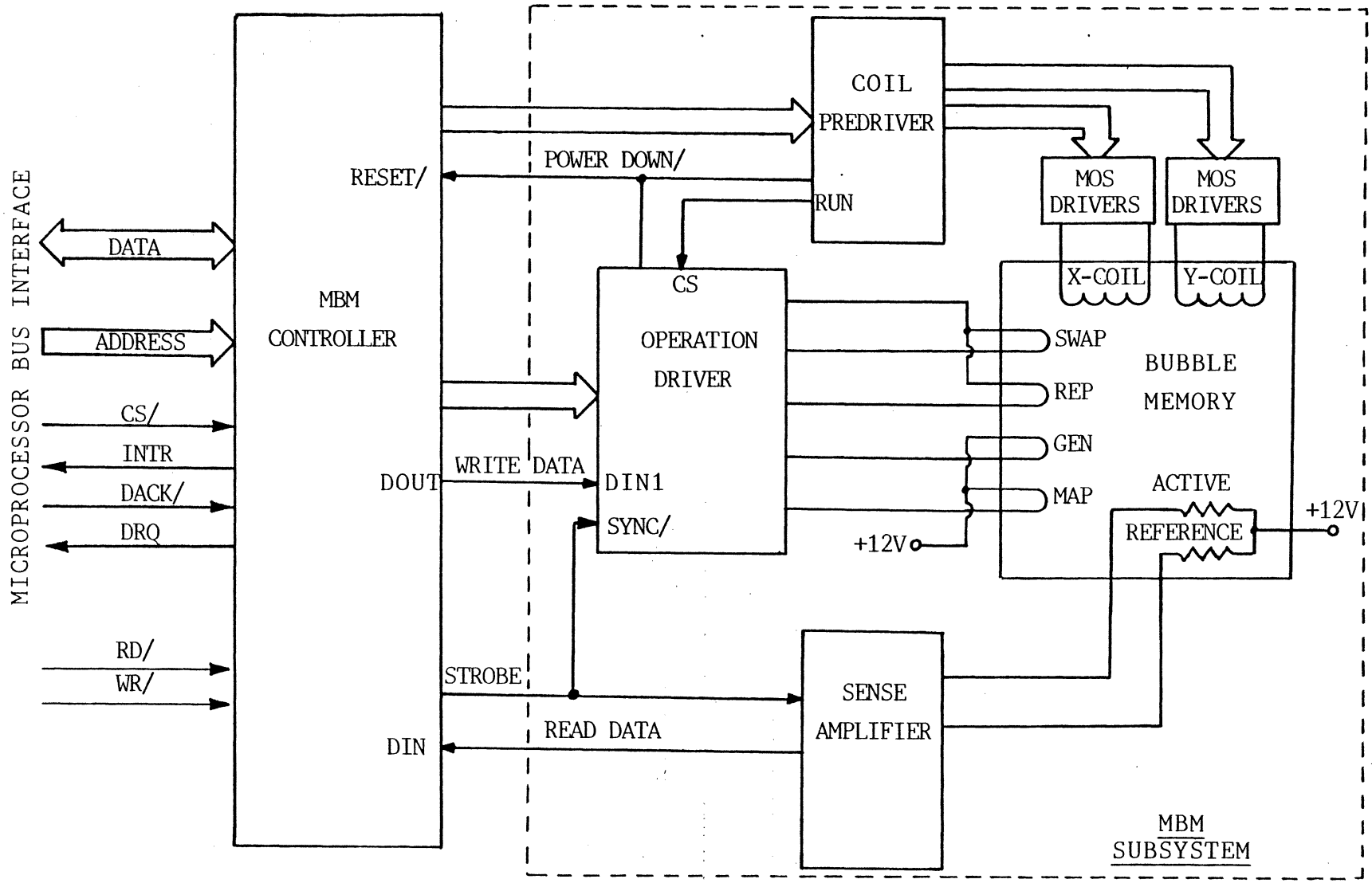


FIGURE 2.4

BUBBLE MEMORY SYSTEM FUNCTIONAL BLOCK DIAGRAM

CHAPTER 3

COMPONENTS OF THE BUBBLE MEMORY SYSTEM

The purpose of this chapter is to describe in detail the organizations of Motorola's MBM2256 256 kilobit and MBM2011 one megabit bubble memory devices as well as the designs of the peripheral integrated circuits which service them.

3.1 THE MAGNETIC BUBBLE MEMORY DEVICE

The Motorola MBM2256 and MBM2011 are magnetic bubble memory devices with 262,144 x 1 (i.e., 2^{18}) bits and 1,048,576 x 1 (i.e., 2^{20}) bits, respectively, of user memory capacity. Externally, they differ only in total user memory capacity and function current amplitude and timing requirements. Both bubble memory devices are of block swap/replicate architecture, but the MBM2256 is organized in a dual arrangement with the two generate elements connected in series and a double period spacing between minor loops. Both the MBM2256 and MBM2011 bubble memory devices are shown in Figure 3.1.

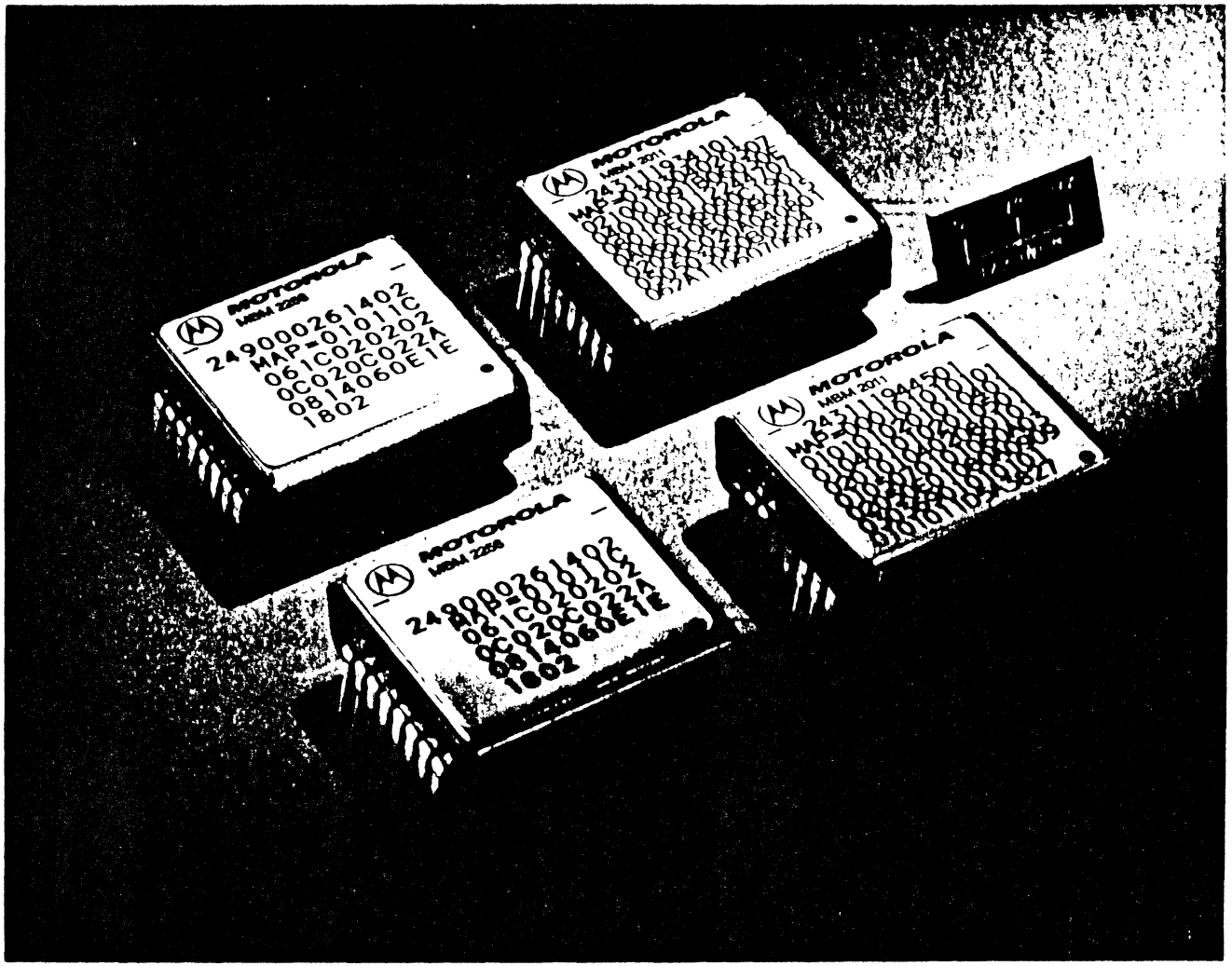


FIGURE 3.1

MOTOROLA BUBBLE MEMORY DEVICES

3.1.1 The MBM2256

The 256 kilobit MBM2256 memory device is a non-volatile, solid-state bubble memory with 262,144 bits of user memory capacity. It is packaged in a 16-pin dual-in-line package measuring only 1.15 x 1.10 x 0.36 inches. The device comes equipped with all the necessary magnetic components including the X and Y drive field coils, required for bubble propagation, the permanent magnets required for non-volatile operation, and a magnetic shield casing that is capable of shielding external magnetic fields of up to twenty oersteds. An assembly diagram of the bubble memory device is depicted in Figure 2.1 Section 2.1. A Z coil is also provided which allows for bulk erase capability or for modulating the bias field intensity (useful in wide temperature applications).

The block diagram of Figure 3.2 shows the basic internal organization of the MBM2256. Note that the minor loops are arranged in a dual block swap/replicate organization with the odd numbered minor loops located on one side of the die and the even numbered minor loops on the other. The two generate gate elements are connected in series and provide duplicate write data to both halves of the die. However, the double period spacing provided between adjacent minor loops results in the even data bits being aligned between the odd numbered minor loops on one-half

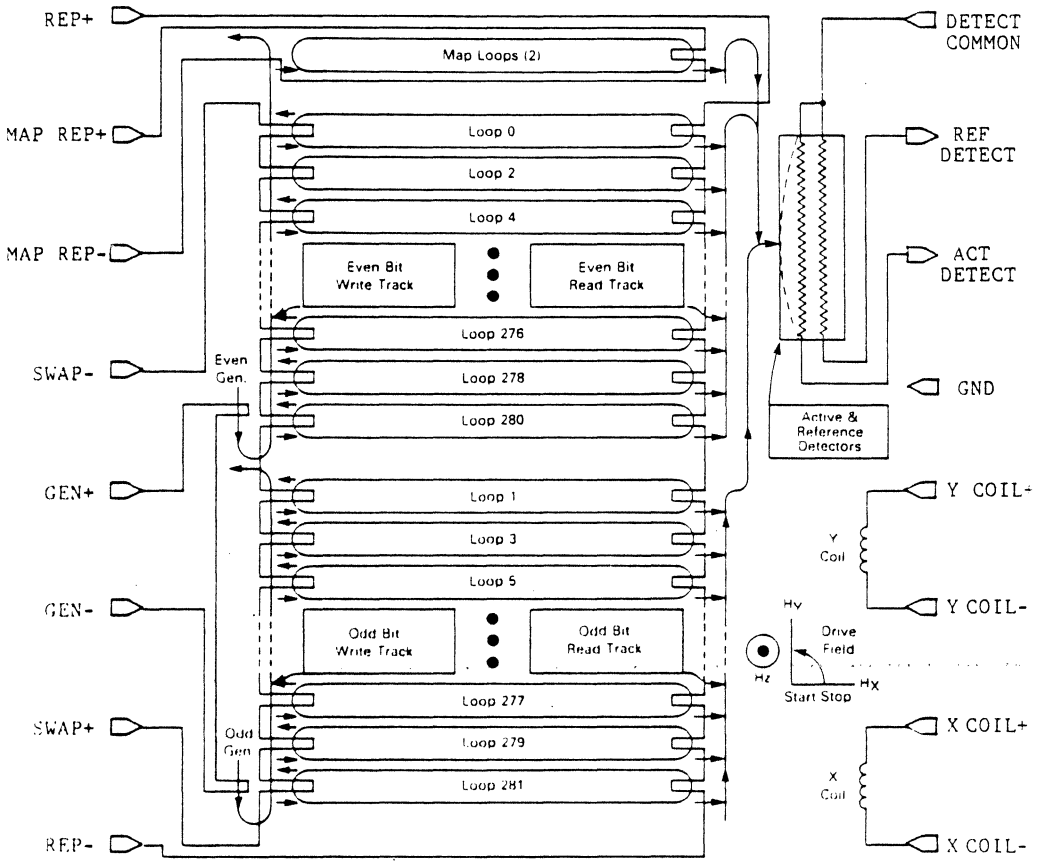


FIGURE 3.2

THE MBM2256 BUBBLE MEMORY

of the die and the odd data bits being aligned between the even numbered minor loops on the other one-half of the die at the time the data block swap function current pulse is applied. On the other hand, during the data block read operation, odd and even data bits are interleaved on the read track prior to entering the detector region.

There are a total of 282 minor loops and 2 map loops provided on the bubble memory die with an individual minor loop capacity of 1024 bits (i.e., 1024 cell geometries or periods) each. Only one map loop is used to store the redundancy map information (RMPI), which identifies the minor loops that should not be written to or read from. The best of the two map loops is identified during the device final testing and loaded with the redundancy map information at that time as well as identified on the device label.

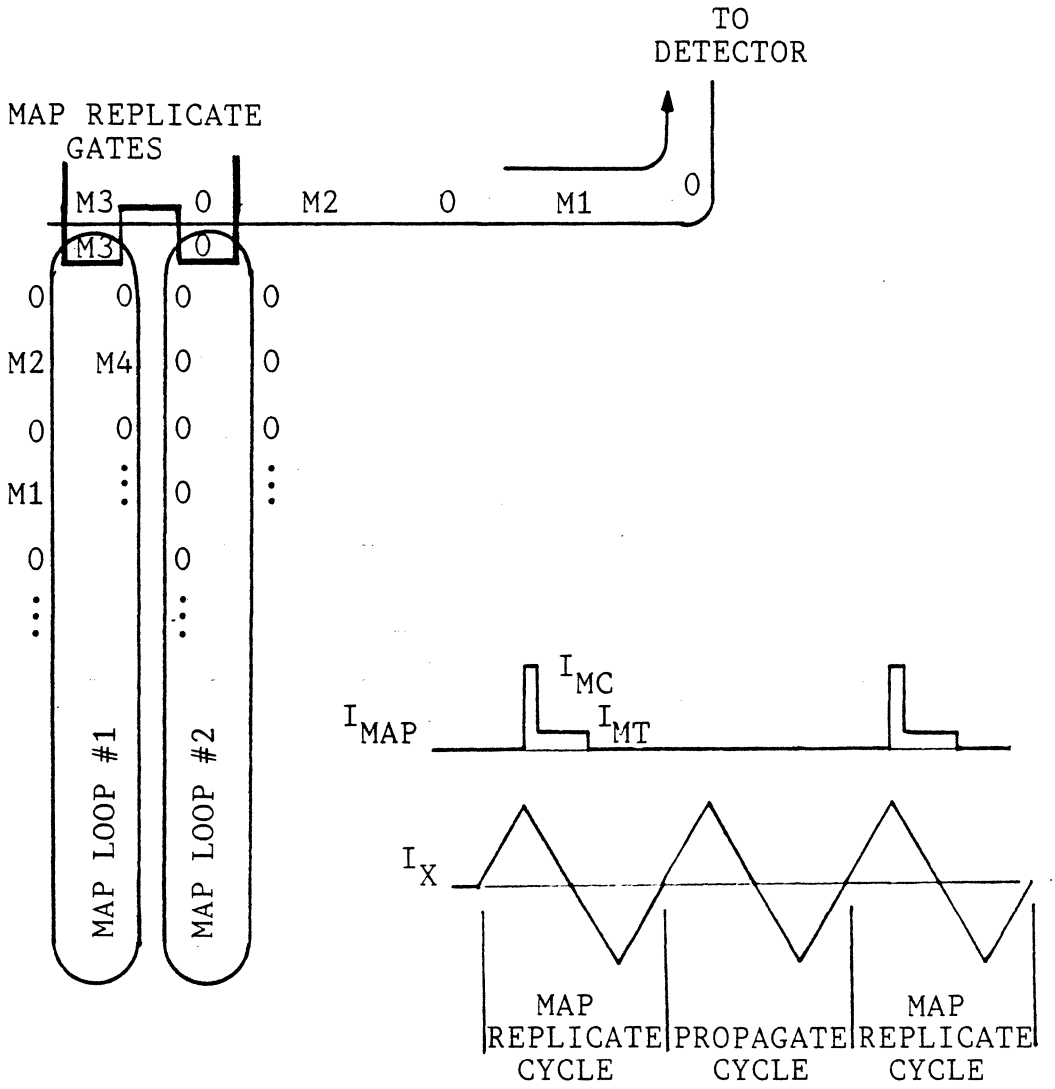
Each map loop is provided with its own replicate gate (although they are connected in series on the die) for reading the RMPI during an MBM system initialization. This information can then be used in formatting the serial write and read data streams of the MBM subsystem.

Because the map replicate function takes place in parallel and on alternate MBM propagation cycles, the redundant map loop as well as alternate bit positions in the loaded map loop must be zeroes to prevent false syn-

chronization. Figure 3.3 shows the structure of map replicate operation. Also stored in the map loop are 12 error detection/correction bits, 2 map loop identifier bits, 150 user bits and a 66-bit synchronization pattern. The synchronization pattern consists of 64 zeroes followed by a one, which is followed by either a one or zero. Care must be exercised in ensuring that the synchronization pattern is not duplicated.

As a result, the map loop read operation will result in a serial data stream being read by way of the bubble memory detector bridge as shown in Figure 3.4.

Of the 282 minor loops, the best 262 are identified during the device final test. Of the 262 best loops, 256 are used for data storage, while 6 remaining minor loops are used for error correction code bits. (Since the SC42584 256K MBM controller uses 12-bit Fire code appended to a 512 bit data block, the minimum one-device read and write operation requires two block replicates and two block swaps, respectively.) The information pertaining to which loops are declared redundant and subsequently are to be formatted out of the serial write and read data streams is encoded onto the device label as well as stored in the map loop.



NOTE: Map loop #1 is loaded with the RMPI and Map loop #2 is redundant in this illustration.

FIGURE 3.3

READING THE MAP LOOPS

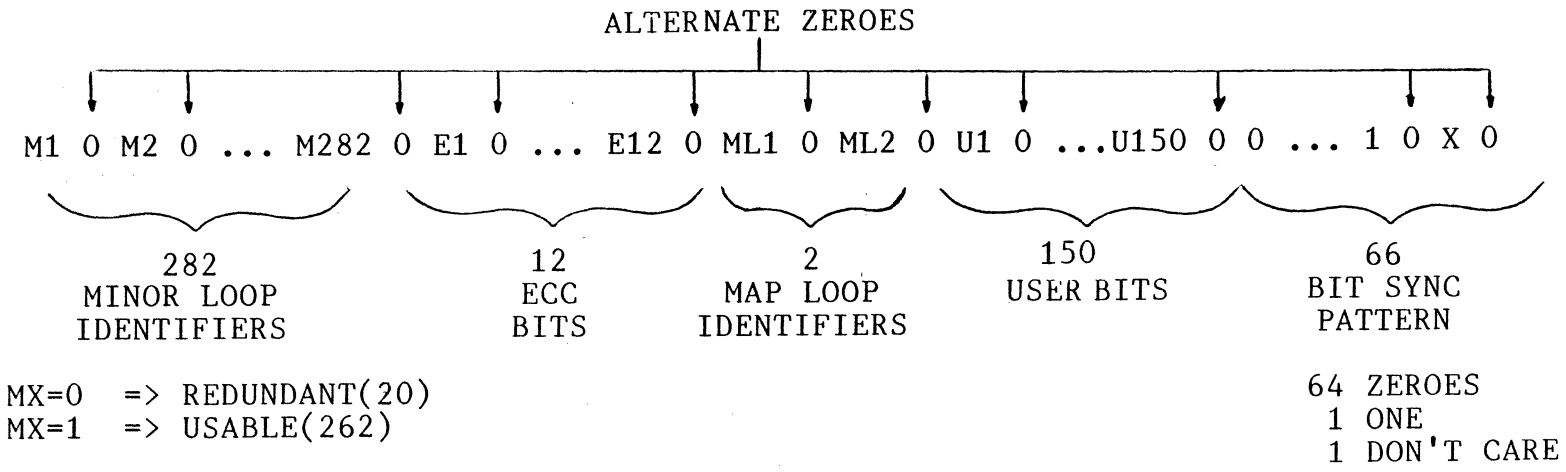


FIGURE 3.4

MBM2256 MAP LOOP DATA FORMAT

The detector stack is composed of an active and a reference (or dummy) magnetoresistive element to allow for differential amplification and detection of the resulting voltage signals. A bubble domain stretcher is located adjacent to the active detector element and acts to stretch the bubble domains entering the detector region from cylindrical to long strips in order to amplify their effect upon the magnetoresistive detector element. A guard rail located between the active and reference detector elements annihilates the bubble domains leaving the active detector element and prevents bubbles from crossing the reference detector element.

The MBM2256 is designed to operate at a drive field frequency of 125 KHz, resulting in a maximum data transfer rate of 125 kilobits per second and an average access time of 6.9 milliseconds.

3.1.2 The MBM2011

The one megabit MBM2011 memory device is a non-volatile, solid-state bubble memory with 1,048,576 bits of user memory capacity. It is pin-compatible with the MBM2256 and is packaged in a 16-pin dual-in-line package measuring only 1.15 x 1.10 x 0.36 inches (same as the MBM2256). The device comes fully equipped with all the necessary magnetic components shown in Figure 2.1 Section 2.1. A Z coil is also

provided which allows for bulk erase capability or for modulating the bias field strength.

The block diagram of Figure 3.5 shows the basic internal organization of the MBM2011. Note that the architecture is a block swap/replicate organization with minor loop arranged sequentially, unlike the dual organization of the MBM2256 (although externally, both the MBM2011 and MBM2256 appear the same).

A single generate gate element nucleates bubble domains (corresponding to logic '1') on a single write track. When data are aligned (i.e., when the first data bit generated reaches minor loop zero located at the far end of the write track), a single data swap function current diverts the write data into all the minor loops, while the old data is dumped out from the minor loops onto the write track.

Likewise, the data read operation requires only a single data replicate function current for data to be sent to the MBM detector by way of the read track.

Each minor loop is provided with its own swap and replicate gate located on opposite sides of the loop. All minor loop replicate gates and all minor loop swap gates are connected in series to faciliate the block read and block write operations, respectively, from all minor loops in parallel.

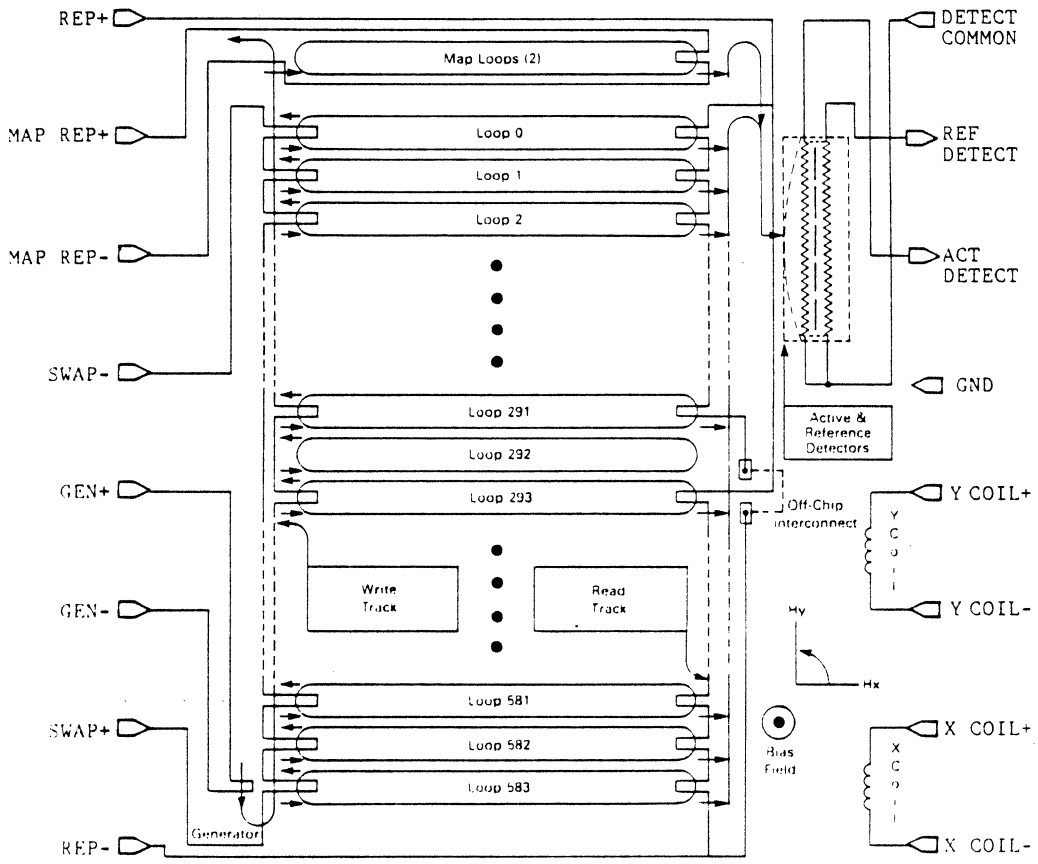


FIGURE 3.5

THE MBM2011 BUBBLE MEMORY

There are a total of 584 minor loops and 2 maploops provided on the MBM2011 bubble memory die with an individual minor loop capacity of 2048 bits each. Like the MBM2256 only one maploop is used to store RMPI. The maploop read operation also takes place in a manner similar to that of the MBM2256, although the field length differs as shown in Figure 3.6.

Of the 584 minor loops, the best 524 are identified during final test. Of the 524 best loops, 512 are used for data storage while the remaining 12 are reserved for error detection/correction bits.

Like the MBM2256, the one megabit MBM2011 is equipped with an active and reference magnetoresistive detector element to allow for differential amplification and detection of bubble signals. A stretcher is provided to amplify the magnetic effects of the bubble domains upon the detector elements. A guard rail is also provided to prevent domains from crossing the reference detector element.

The MBM2011 is designed to operate at a drive field frequency of 100KHz, resulting in a maximum data transfer rate of 100 kilobits per second and an average access time of 11.2 milliseconds.

Table 3.1 summarizes the characteristics of the MBM2256 and MBM2011.

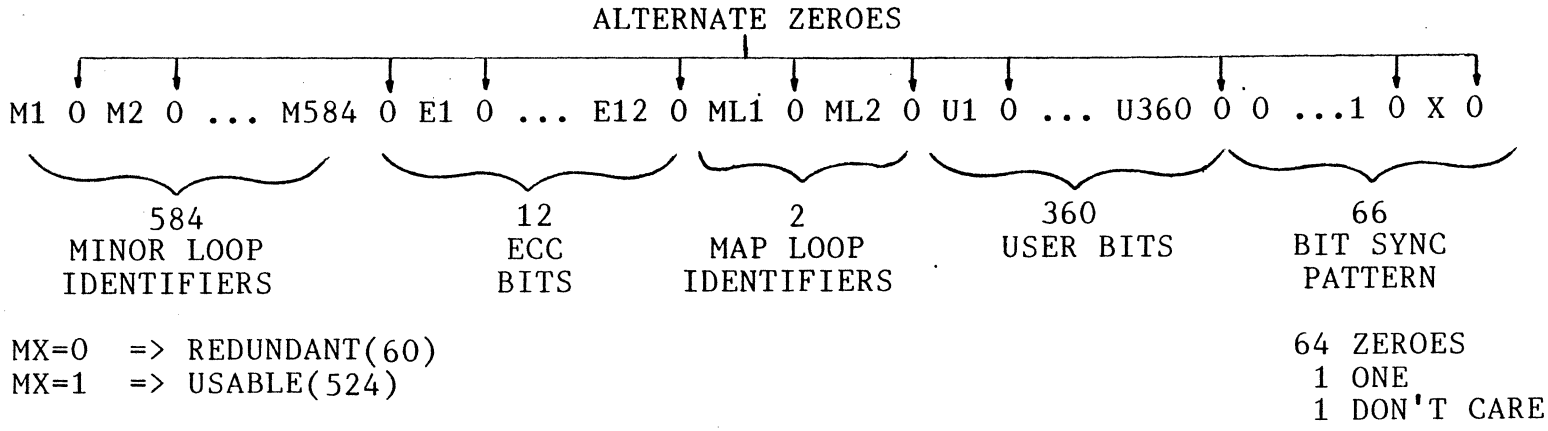


FIGURE 3.6

MBM2011 MAP LOOP DATA FORMAT

CHARACTERISTIC	MBM 2256	MBM2011
Memory capacity (bits)	262,144	1,048,576
Memory organization	Dual block swap/rep. 262,144 x 1	Block swap/rep. 1,048,576 x 1
Number of minor loops	282	584
Usable minor loops	262	524
Redundant minor loops	20	60
Number of maploops	2	2
Redundant maploops	1	1
Minor loop capacity (bits)	1024	2048
Die size ($mils^2$)	313 x 331	400 x 404
Bubble size (microns)	3	2
Operating frequency (KHz)	125	100
Maximum data rate (Kbits/s)	125	100
Average access time (mS)	6.9	11.2
Non-volatile storage (°C)	-40 to 100	-40 to 100
Package dimensions (in^3)	1.15 x 1.10 x 0.36	1.15 x 1.10 x 0.36
Number of pins	16	16
Package weight (g)	28	28
Magnetic shield capability (Oe)	20	20

TABLE 3.1

MBM2256 and MBM2011 DEVICE CHARACTERISTICS

3.2 THE MBM CONTROLLER

The SC42584 and SC42585 MBM Controllers are 40-pin monolithic HMOS integrated circuits designed for use with Motorola's MBM2256 (256 Kb) and MBM2011 (1 Mb) bubble memory devices, respectively. They are functionally identical and differ only in bubble memory subsystem control timings, nominal crystal frequency and data record lengths. Their primary functions are (1) to provide a user interface to the bubble memory subsystem and manage the data handling functions including redundant loop management, (2) to process all commands, (3) to manage all the timing requirements of the bubble memory subsystem, and (4) to perform the tasks of error detection and correction. In addition, both MBM controllers also have the capability of operating 2, 4, or 8 bubble memory subsystems in parallel. In these cases, the data transfer rate multiplies from the single MBM data transfer rate by the number of MBMs operating in parallel (as does the total system memory capacity). See Chapter 4 for a more detailed discussion regarding parallel operation of bubble memories.

3.2.1 User Interface and Data Handling

The SC42584 and SC42585 bubble memory controllers provide the hardware and software interface between a user's system and the bubble memory subsystem. The standard 8-bit

microprocessor bus structure of the controllers is designed to directly interface with most microprocessor-based systems. The 8-bit data bus carries commands, data, status, and system control information between the user system and the bubble memory system. A block diagram of the MBM controller is shown in Figure 3.7.

The programming model for the MBM controller is given in Figure 3.8. The user has access to seven internal registers or the data FIFO. With the exception of the Status Register (read-only), the registers and data FIFO are read/write registers. To access a particular register or the data FIFO, the user system presents the appropriate address on address lines AØ-A2 and activates CS/ and RD/ or WR/ (depending upon whether the register is to be read from or written to, respectively). If the access operation is a write operation, the valid data to be stored must also be presented on the data bus (DØ-D7) simultaneously. In the case of a read operation, the MBM controller presents data on the data bus corresponding to that stored in the register or FIFO buffer. Figure 3.9 illustrates the interface timing requirements of the MBM controller.

The Command Register (CMDR) is an 8-bit register which accepts valid commands presented on the user interface and commences command execution upon accepting the command

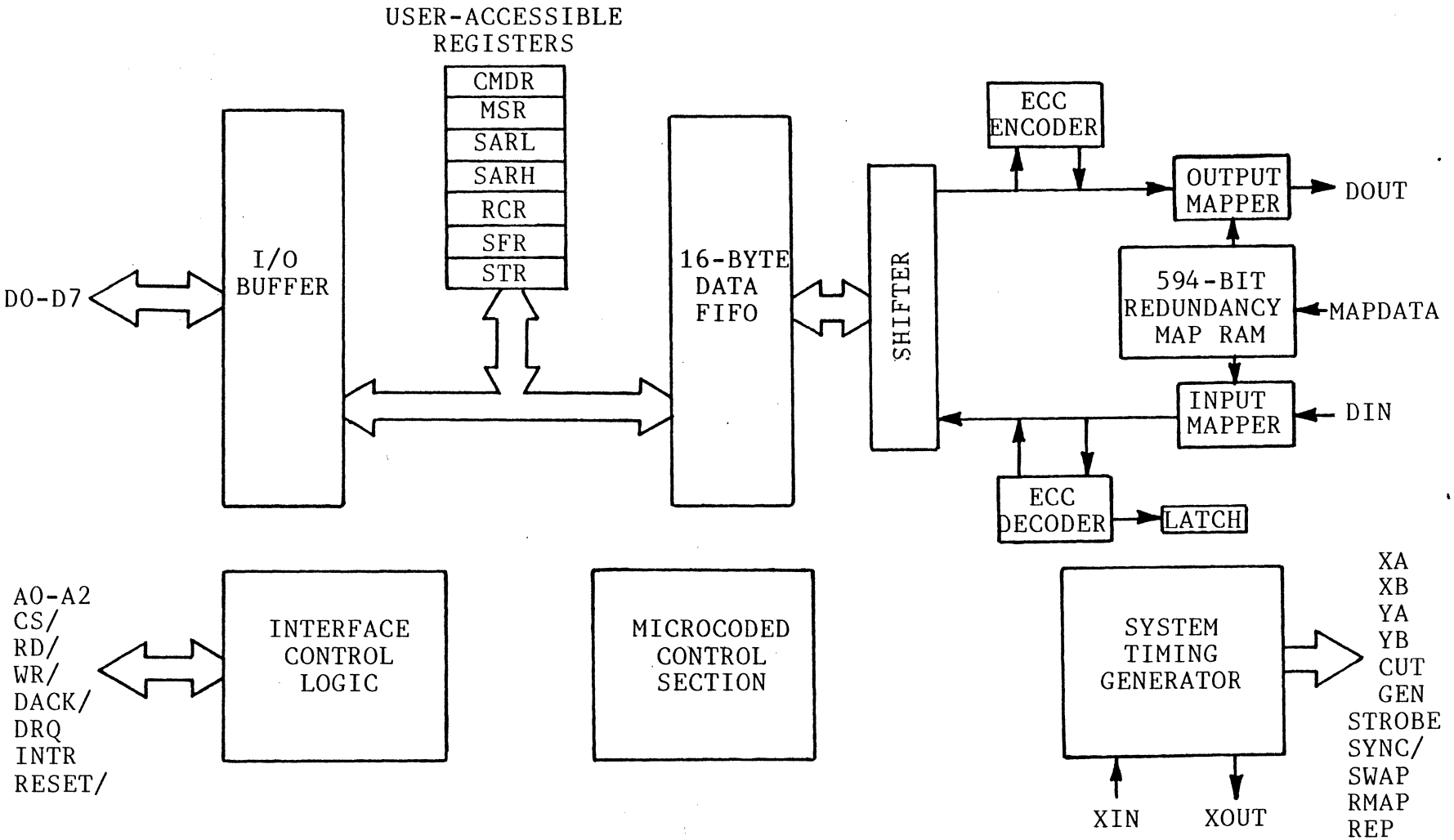


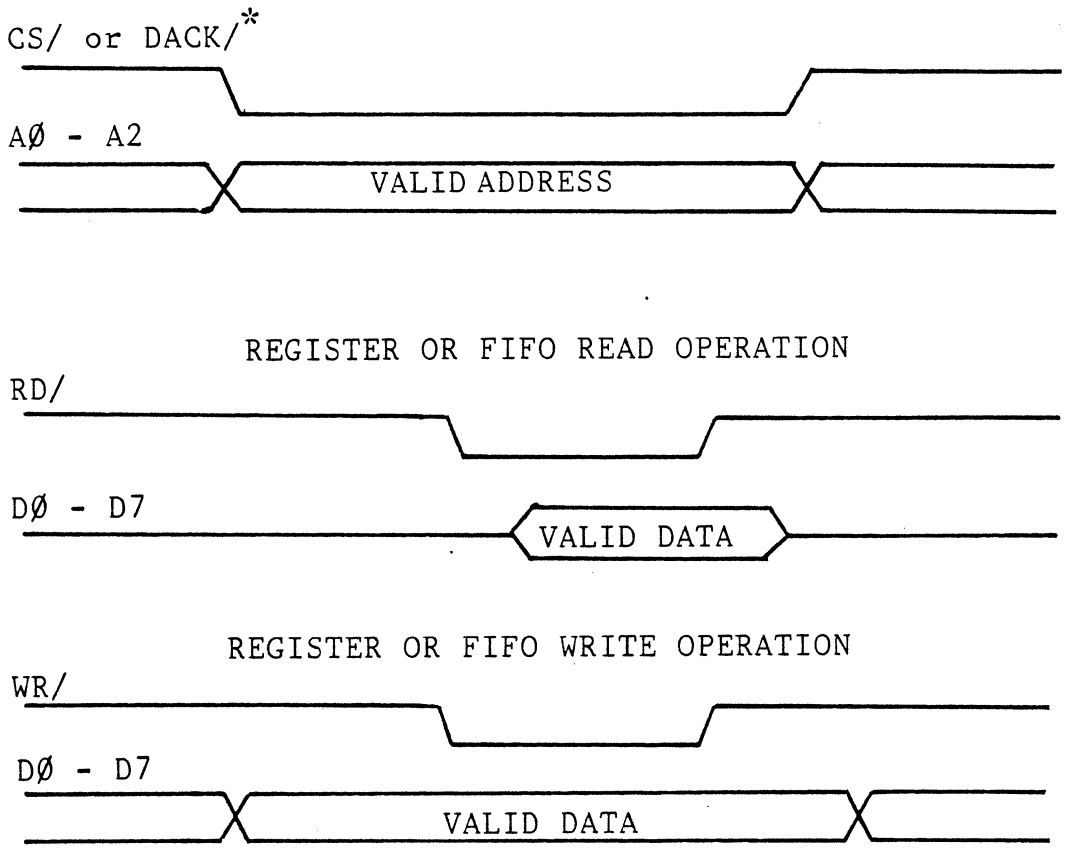
FIGURE 3.7

MBM CONTROLLER BLOCK DIAGRAM

ADDRESS A2 A1 A0		ACCESS
0 0 0	COMMAND REGISTER (CMDR)	R/W
0 0 1	MULTIPLE SECTOR REGISTER (MSR)	R/W
0 1 0	SECT ADDR REGISTER - LOW (SARL)	R/W
0 1 1	SECT ADDR REGISTER - HIGH (SARH)	R/W
1 0 0	RESIDUAL CONTROL REGISTER (RCR)	R/W
1 0 1	SYSTEM FEATURES REGISTER (SFR)	R/W
1 1 0	STATUS REGISTER (STR)	READ-ONLY
1 1 1	FIFO BUFFER (FIFO)	R/W

FIGURE 3.8

MBM CONTROLLER PROGRAMMING MODEL



*DACK/ is activated by a DMA controller during DMA transfers with the data FIFO.

FIGURE 3.9

MBM CONTROLLER INTERFACE TIMING

byte. The various commands that can be executed are discussed in Section 3.2.2.

The Multiple Sector Register (MSR)is an 8-bit register used during the execution of multiple page/sector (selectable in the RCR) commands and indicates the number of pages/sectors to be transferred. During execution, the MSR is decremented following the transfer of every page/sector. If the STOP ON ERROR option is selected (selectable in the RCR) and a read error is detected in one of the pages/sectors the MSR will contain the number of pages/sectors remaining to be transferred including the one in error. This register is not used during the execution of single page/sector transfers.

The Sector Address Register (SAR) is used to address a page/sector of data. The SAR is an 11-bit register in which the low-order SARL is 8 bits and the high-order SARH is 3 bits. If necessary, the user loads the SAR prior to loading the command register. The SAR is automatically incremented following execution of a command on a record of data.

The Residual Control Register (RCR) is a 7-bit register which is used to select the various options available in the MBM controller. A description of the RCR option bits is given in Figure 3.10.

RESIDUAL CONTROL REGISTER

BIT	7	6	5	4	3	2	1	Ø
	NOT USED	READ BUFFER ENABLE	STOP ON ERROR	HALF BUFFER	ENABLE READY INTR	ENABLE DRQ INTR	PAGE MODE	WRITE PROTECT

READ BUFFER ENABLE: When set to 1 allows the data FIFO to be read when no command is being executed. If set to Ø the data FIFO may only be written to when no command is being executed. Used primarily for diagnostic purposes.

STOP ON ERROR: Forces the controller to halt data transfer at the current ECC block when an error is detected in the data. The ECC logic, MSR, and SAR are left in the proper state to reread or execute a READ CORRECTED.

HALF BUFFER: Causes DRQ to be set when the FIFO is at least half empty during a write operation or at least half full during a read operation. 8-byte burst transfers can therefore be made.

ENABLE READY INTERRUPT: Causes INTR to be activated at the completion of any command. INTR is then cleared by reading the status register.

ENABLE DRQ INTERRUPT: Causes INTR to be activated when DRQ is active.

PAGE MODE: Set to 1 implies page addressing.
Set to Ø implies sector addressing.

WRITE PROTECT: Prevents the execution of any WRITE command when set to 1.

FIGURE 3.10

RESIDUAL CONTROL REGISTER DESCRIPTION

The System Features Register (SFR) is a 3-bit register used to inform the controller of the bubble memory subsystem configuration. A description of the SFR bits is given in Figure 3.11.

The Status Register (STR) is an 8-bit read-only register used to indicate to the user system the status of the command in progress or last executed. This register is cleared when a command is loaded into the CMDR or following a system reset. A description of the Status Register bits is given in Figure 3.12.

The data FIFO is a 16-byte buffer used to absorb the timing differences between the bubble memory subsystem and the user's system. Logically, it is organized as a ring buffer and handles all read and write data. During a bubble memory WRITE operation, the controller requests data by setting the hardware DRQ line and STR bit 1 (DRQ) to one, indicating to the user that one or more memory locations in the FIFO are available to accept a data byte. Likewise, during a READ operation, the controller sets the hardware DRQ line and STR bit 1 (DRQ) to one to indicate that at least one byte of data has been assembled in the FIFO and can be read by the user.

SYSTEM FEATURES REGISTER

BIT	7	6	5	4	3	2	1	Ø
	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	EXT MAP	NM1	NMØ

EXT MAP: Signals the controller not to use its internal MAP RAM for storage of the RMPI. The controller then assumes that the RMPI is stored in an external RAM or PROM.

NM1 and NMØ: Defines for the controller the system configuration. In particular, these bits specify the number of bubble memory devices operating in parallel.

NM1	NMØ	
Ø	Ø	1 MBM
Ø	1	2 MBMs
1	Ø	4 MBMs
1	1	8 MBMs

FIGURE 3.11

SYSTEM FEATURES REGISTER DESCRIPTION

STATUS REGISTER

BIT	7	6	5	4	3	2	1	Ø
	SOFT ERROR	WRITE PRO-TECTED	IERR/ MCERR/ ORERR	NON-COR-RECTABLE ERROR	DATA ERROR	OVER-RUN ERROR	DRQ	READY

NOTE: STR7 & STR6 both 1 indicates that a RESET is pending.

SOFT ERROR: Indicates that the recomputed syndrome of the READ CORRECTED command did not match the previous syndrome.

WRITE PROTECTED: Indicates that the WRITE PROTECT bit (RCRØ) is set and the attempted WRITE command was not executed.

IERR/MCERR/ORERR: Following an INITIALIZE command indicates that an initialization error was encountered in that the synchronization pattern was not found.

Following a MAP READ command indicates that the data read from the map loop did not match what is stored in the MAP RAM.

Following a READ or WRITE DATA command indicates the the page/sector was out of range for the number of MBMs specified.

NON-CORRECTABLE ERROR: Following a READ CORRECTED command indicates that the error is non-correctable.

DATA ERROR: Following a READ command indicates that a data error was detected.
Following a READ CORRECTED command indicates that an error in another ECC block was detected.

OVERRUN ERROR: Indicates that a data buffer overrun occurred. Results when the user system fails to keep up with the MBM system data transfer rate or when a read or write to the buffer was attempted when DRQ = Ø.

DRQ: Data transfer request. Used to indicate that data is available in the data buffer (FIFO) during a READ operation or that there is room in the data buffer during a WRITE operation.

READY: Indicates that the previous command execution has been completed and that the controller is ready to accept a new command

FIGURE 3.12

STATUS REGISTER DESCRIPTION

The MBM controllers provide for three methods of transferring data between the user system and the bubble memory system. They are:

*Programmed

*Interrupt-driven

*Direct Memory Access (DMA)

In the programmed-mode of operation, the user continuously reads the status register and determines if DRQ (STR bit 1) or READY (STR bit Ø) are set. In the case of DRQ=1, the user transfers data to/from the data FIFO. In the case of Ready=1, the user is informed that the previous command execution has been completed and that the other bits in the STR can now be polled to determine if any errors were encountered.

The MBM controller can be programmed to set the hardware INTR line to one upon the completion of a command and/or when data is to be transferred to/from the data FIFO by setting the RCR bit 3 and bit 2, respectively. Setting RCR3=1 causes the controller to interrupt the user system when the previous command has completed execution. A read to the status register resets the INTR line. Setting RCR2=1 causes the controller to interrupt when data is assembled in the FIFO during a READ operation or when space is available in the FIFO during a WRITE operation. The interrupt-driven method of data transfer is usually less of a burden

on the user system than is the programmed-mode simply because the user system does not have to continuously be reading the STR, instead it can be tending to other duties.

Two hardware lines, DACK/ and DRQ are provided at the controller interface to facilitate the handshaking operations of a DMA transfer when the user provides a DMA controller. Activating DACK/ allows access directly to the data FIFO regardless of the address lines AØ-A2. (For this reason, CS/ must remain inactive during DMA operations.) DRQ is set to one when data is available in the FIFO during a bubble memory READ operation or when space is available in the FIFO during a bubble memory WRITE operation.

In the case of a READ, the DMA controller (after gaining control of the system bus) responds to DRQ by setting RD/ and DACK/ to zero and subsequently, reading the data bus. The controller responds to DACK/ and RD/ by putting a byte from the FIFO onto the data bus.

Likewise, in the case of a WRITE, the DMA controller responds to DRQ active by gaining control of the system bus and issuing a DACK/ and WR/ along with the data to be stored in the bubble memory. The controller responds to DACK/ and WR/ by latching the data from the data bus and loading it into the FIFO.

Two basic record lengths of data can be established for the MBM controllers - pages or sectors. (Multiple page/sector transfers can also be established.) A page of data is defined as the data length resulting from a single data replicate operation. (The exception to this rule is the one-device 256 Kbit bubble memory system in which two data replicates must be performed to fulfill the 512 bit requirement of the ECC block.) Therefore, the page size increases as the number of MBMs operated in parallel is increased. On the other hand, a sector of data is defined as the data page length resulting from eight bubble memories operating in parallel. Table 3.2 lists the data lengths for the SC42584 and SC42585 for various system configurations.

The MBM controller also handles the parallel-to-serial/serial-to-parallel conversions of data from/to the data FIFO and the redundant loop management as required by the bubble memory subsystem. During the execution of a WRITE DATA command, the controller takes data bytes from the FIFO and shifts the data serially to the output mapper. The output mapper, in turn, consults the RMPI stored in the MAP RAM (and external RAM or PROM, if necessary) and inserts zeroes in the write data stream corresponding to the redundant loops, thereby preventing any data from ever being written into bad minor loops.

CONTROLLER	RECORD TYPE	# MBMs IN PARALLEL 1	2	4	8
SC42584	PAGE (bits)	512*	512	1024	2048
	SECTOR (bits)	2048	2048	2048	2048
SC 42585	PAGE (bits)	512	1024	2048	4096
	SECTOR (bits)	4096	4096	4096	4096

* To fulfill the requirements of the ECC block length, the 256 Kbit one-device system performs two data replicate operations per page operation.

TABLE 3.2

PAGE AND SECTOR DATA LENGTHS

Conversely, during the execution of a READ DATA command, the controller takes serial data from the bubble memory subsystem and shifts it into the input mapper. The input mapper, in turn, consults the RMPI and removes the redundant zeroes from the input data stream. Following every eighth data bit, the controller latches the data byte into the FIFO and sets DRQ=1.

The on-chip MAP RAM is 594 bits. Consequently, when multiple bubble memories are operated in parallel, the additional RMPI is diverted to external RAM. Four control signals are provided for this purpose

3.2.2 MBM Controller Commands

The user controls the operation of the MBM system by reading from and writing to the user-accessible registers of the MBM controller. Execution of bubble memory operations is commenced upon writing a command byte to the CMDR. Commands should be written to the CMDR only when READY=1, indicating that no command is currently being executed. The exception to this is the TERMINATE commands which will be accepted by the controller at any time. A summary of the available MBM commands and their associated options is given in Table 3.3. Flow charts detailing the use of the commands are given in Figures 3.13 - 3.20.

COMMAND	FUNCTION PERFORMED	OPTIONS
INITIALIZE	Synchronizes the MBM system to page zero and loads the RMPI into the MAP RAM.	1. Do not load RMPI
TERMINATE	Terminate the command in progress.	1. Immediately 2. At the end of the current page.
POSITION	Align the specified page (in SAR) for the minimum access time.	1. Position for read 2. Position for write
READ DATA	Read a page/sector of data from the MBM.	1. w/o RMPI format 2. Suppress transfer 3. Multiple page/sector
WRITE DATA	Write a page/sector of data to the MBM.	1. w/o RMPI format 2. Suppress transfer 3. Multiple page/sector
READ CORRECTED	Reread the page in error and apply the error correction to that page.	
READ MAP LOOP	Read the contents of the map loop.	1. Send all data 2. Send RMPI & ECC only
WRITE MAP LOOP	Write the map data to the map loop.	1. Map loop #1 2. Map loop #2
CLEAR LPC	Clear the logical page counter.	

TABLE 3.3

MBM CONTROLLER COMMAND SUMMARY

The INITIALIZE command is used to synchronize the MBM system to page zero in the bubble memory device.

Normally, the RMPI is then stored in the MAP RAM, but an option is available to allow for synchronization and error detection only, without loading the RMPI. The SFR and RCR should be loaded prior to command execution. The initialization process should be performed following a power off-on, after the RESET/ pin is activated or when a new MBM is addressed.

The TERMINATE command is used to suspend execution of the current command. The TERMINATE IMMEDIATE command suspends execution immediately, while the TERMINATE suspends execution at the end of the current page.

The POSITION command is used to align the address specified in the SAR for the minimum access time. After execution of the POSITION command, the SAR should not be reloaded or excessive access times (near maximum) will result.

The READ DATA command allows for the reading of bubble data. The user loads the MSR (if multiple transfers are desired) RCR, and SAR (with the first page/sector to be transferred) before issuing the READ DATA command. Options are also available to inhibit the redundant loop management function and to suppress transfers with the user system.

These two options are, however, used primarily for diagnostic purposes.

The WRITE DATA command allows for the storing of user data into the bubble memory. The user loads the MSR, RCR and SAR before issuing the WRITE DATA command. The same options are available as for the READ DATA command.

The READ CORRECTED command is used to apply the error correction logic to a page of data in which an error was detected. Provided the STOP ON ERROR option is selected, the detection of an error during a READ DATA operation will result in the SAR containing the address of the page/sector in error. The MSR will contain the number of pages/sectors yet to be transferred (in multiple read operations) including the one in error. All that is required by the user is to issue the READ CORRECTED command without disturbing the other registers. Additional errors, uncorrectable errors and soft errors will be flagged by the controller as well.

The READ MAP LOOP command is used to send the RMPI and ECC information to the user. All stored map data including the synchronization pattern and the user information bits can also be sent as an option, but the error detection function is inhibited in this case.

The WRITE MAP LOOP command is used to write the RMPI into the map loop of an MBM. The user must supply the entire field as shown in Figures 3.4 and 3.6 (less the alternate zeroes). In addition, the user must first clear the bubble memory device of all bubble domains by supplying a sufficient Z coil current to force the bubble into the collapse region. Since the controller and MBM operation driver perform a transfer-in function (via a shortened swap pulse which acts as a transfer-in current) to write the map loop, the user must provide a means of routing the shortened-pulse swap current through the map replicator in the reverse direction. This can be easily done using a mechanical switch or relay as shown in Figure 3.21.

The CLEAR LPC command is used to clear the MBM controller logical page counter without having to access the MBMs. This operation, therefore, allows the user to synchronize the system with page zero without using the map loops (e.g., by recognizing a page of data with a unique data pattern).

Another useful application for the CLEAR LPC command would involve the use of the Z coil for quickly clearing the bubble device of all data. Using the EXT MAP option, all RMPI could be stored on an external PROM and the need to rewrite the map loop would therefore be unnecessary.

* INITIALIZE
* INITIALIZE AND LOAD

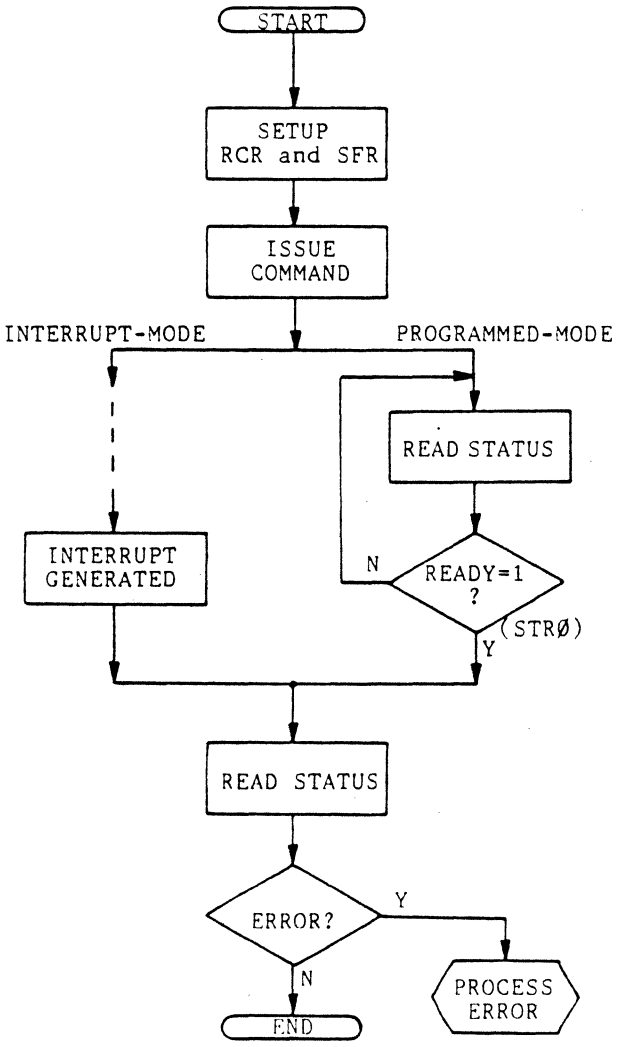


FIGURE 3.13

INITIALIZE COMMAND EXECUTION

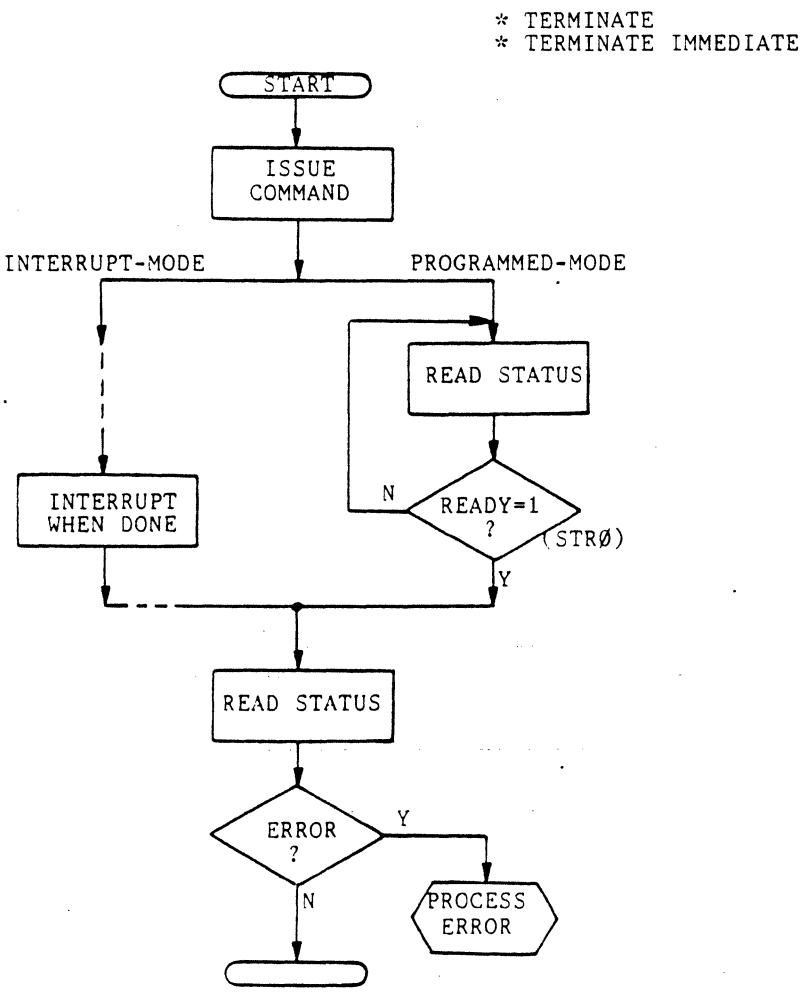


FIGURE 3.14

TERMINATE COMMAND EXECUTION

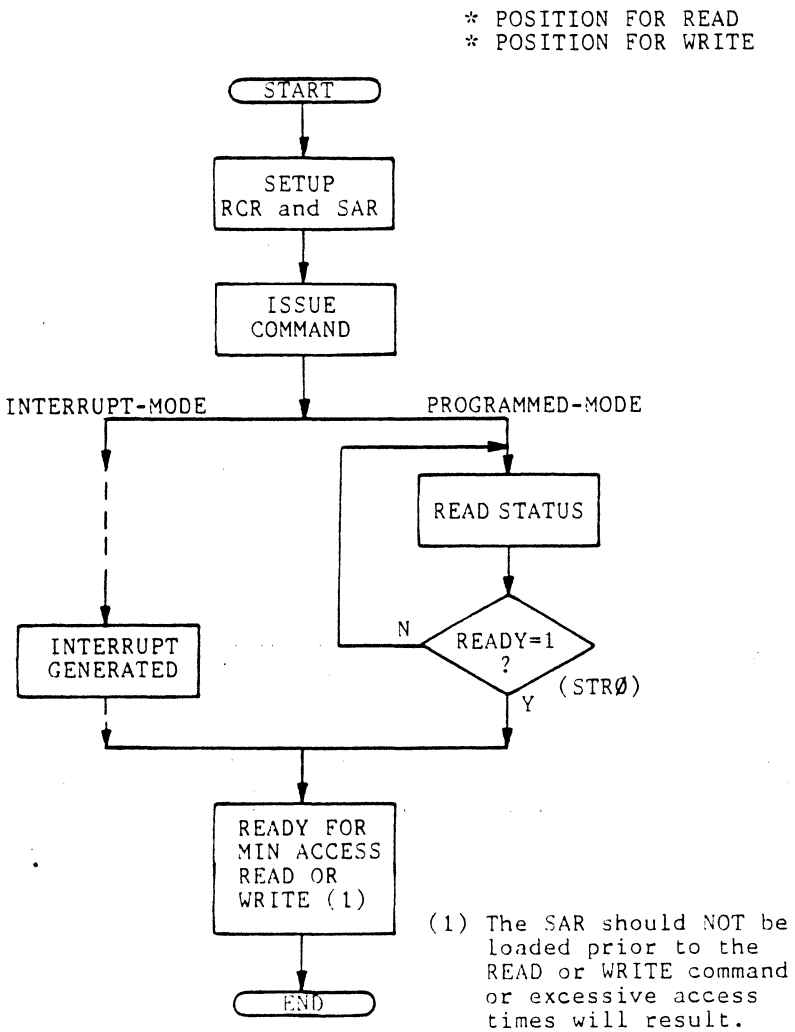


FIGURE 3.15

POSITION COMMAND EXECUTION

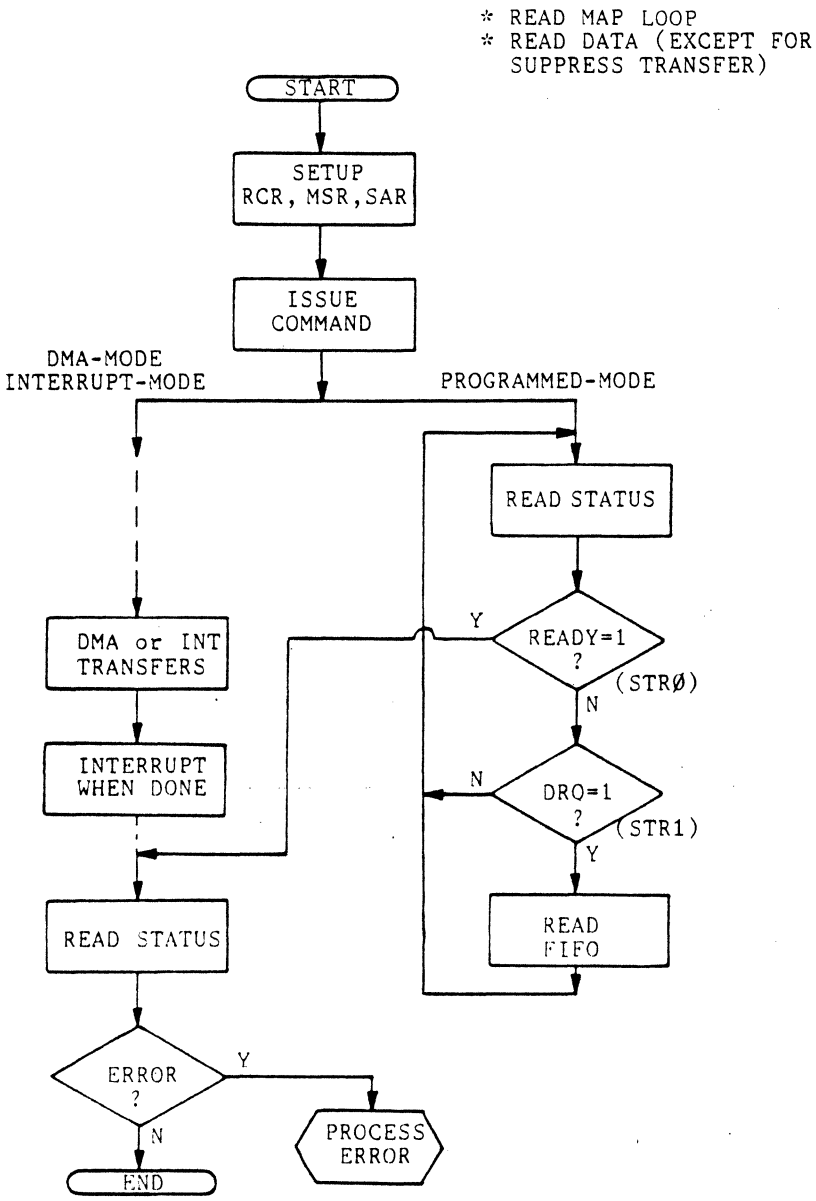


FIGURE 3.16

READ COMMAND EXECUTION

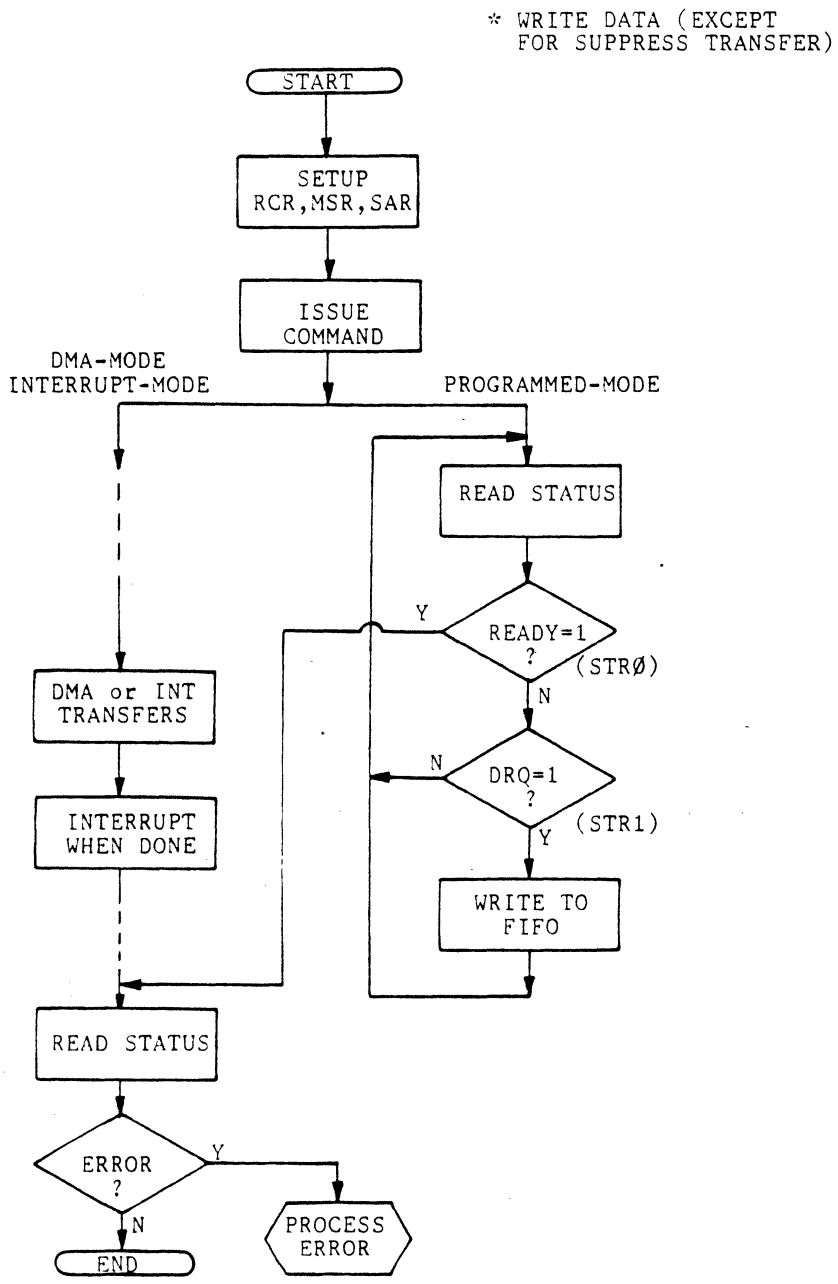


FIGURE 3.17

WRITE DATA COMMAND EXECUTION

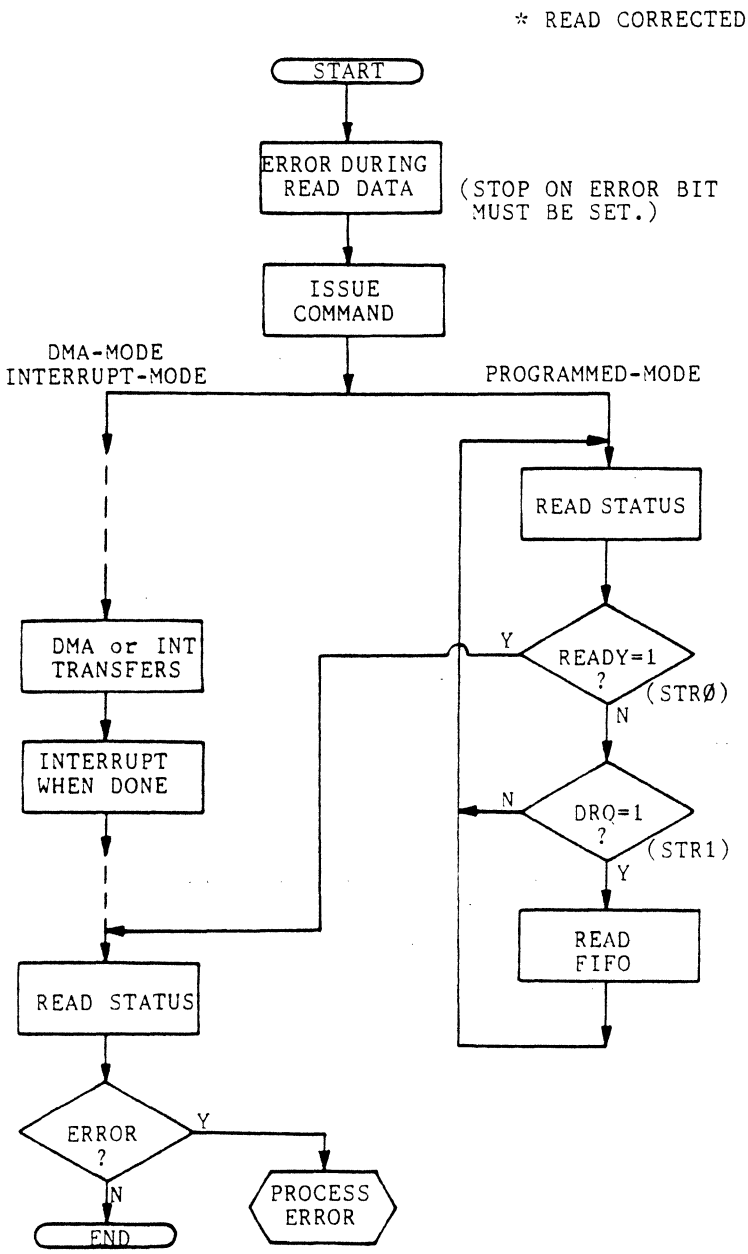


FIGURE 3.18

READ CORRECTED COMMAND EXECUTION

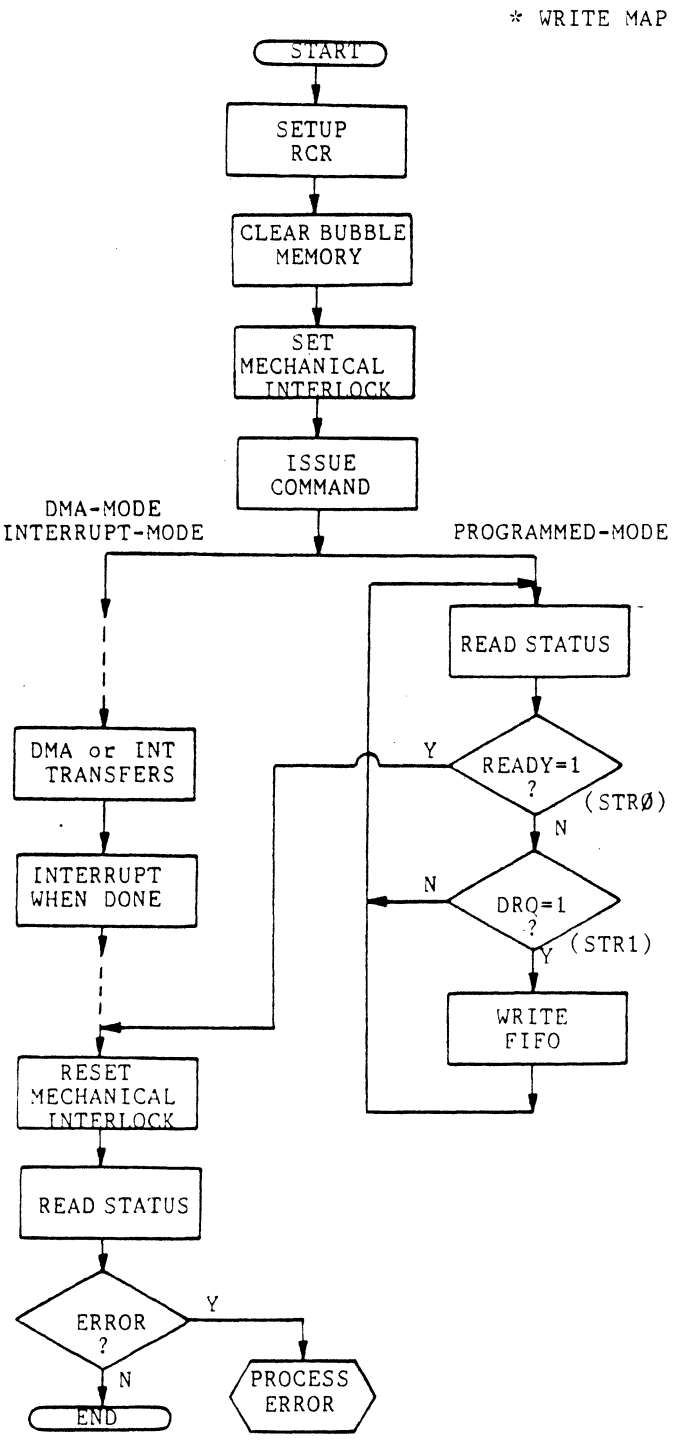


FIGURE 3.19

WRITE MAP COMMAND EXECUTION

* CLEAR LOGICAL PAGE COUNTER

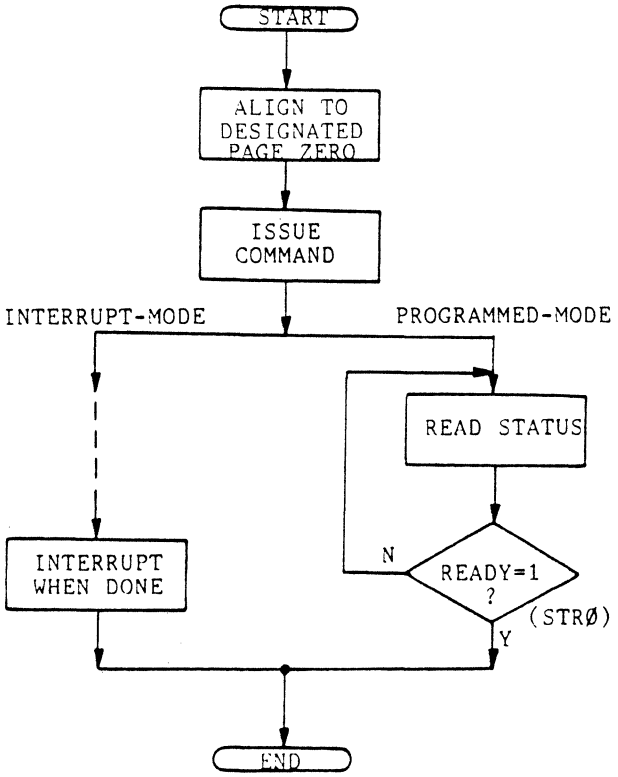
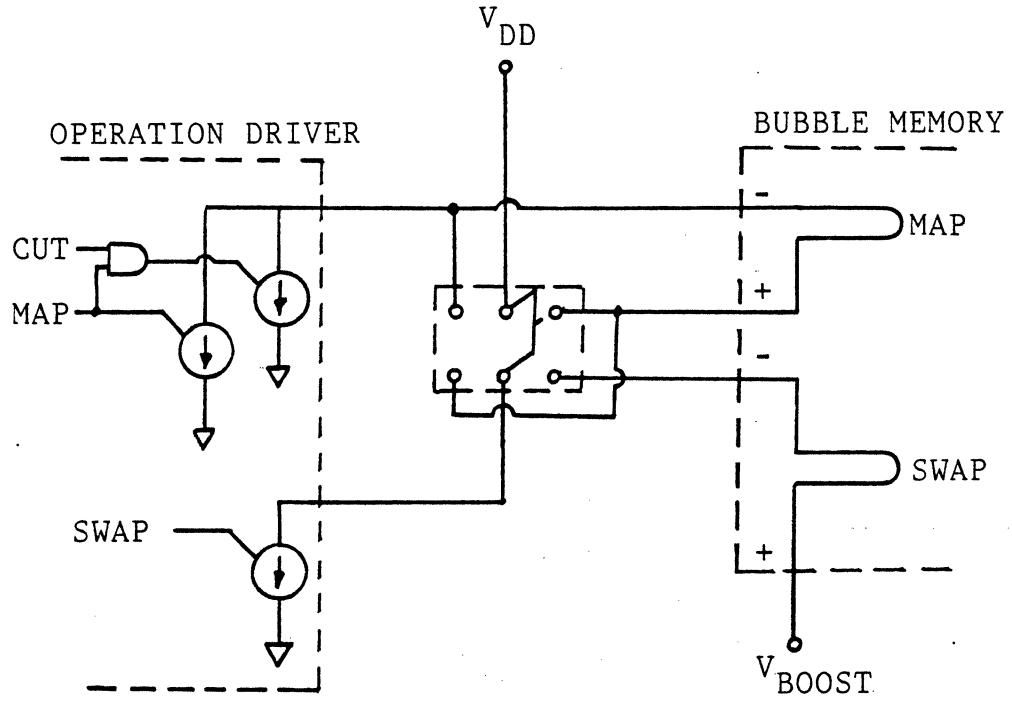


FIGURE 3.20

CLEAR LPC COMMAND EXECUTION



NOTE: Switch thrown to the right for normal operation.
Switch thrown to the left for MAP WRITE.

FIGURE 3.21

MAP WRITE MECHANICAL INTERLOCK

3.2.3 Subsystem Timing Generation

The MBM controller also provides all the addressing management and signal timing generation for the bubble memory subsystem.

Basically, the addressing management function requires that the MBM controller keep track of pages of data with regard to their relative position with respect to the replicate and swap gates. To minimize the write and read access times, the controller assigns sequential page numbers to be separated by slightly more than the entire length of the write track. This results in data being able to be written to sequential addresses during multiple-page write operations almost without pause.

Likewise, during multiple-page read operations, the previous page of data has cleared that portion of the read track in front of the minor loops by the time the next sequential page reaches the replicate gates. Therefore, the following page of data can be replicated onto the read track almost immediately behind the previous page of data.

Since the operation in sector mode is nothing more than multiple-page transfers (with the exception of eight MBMs in parallel), the timing for sector transfers is already established. An example of the megabit addressing scheme is illustrated in Figure 3.22.

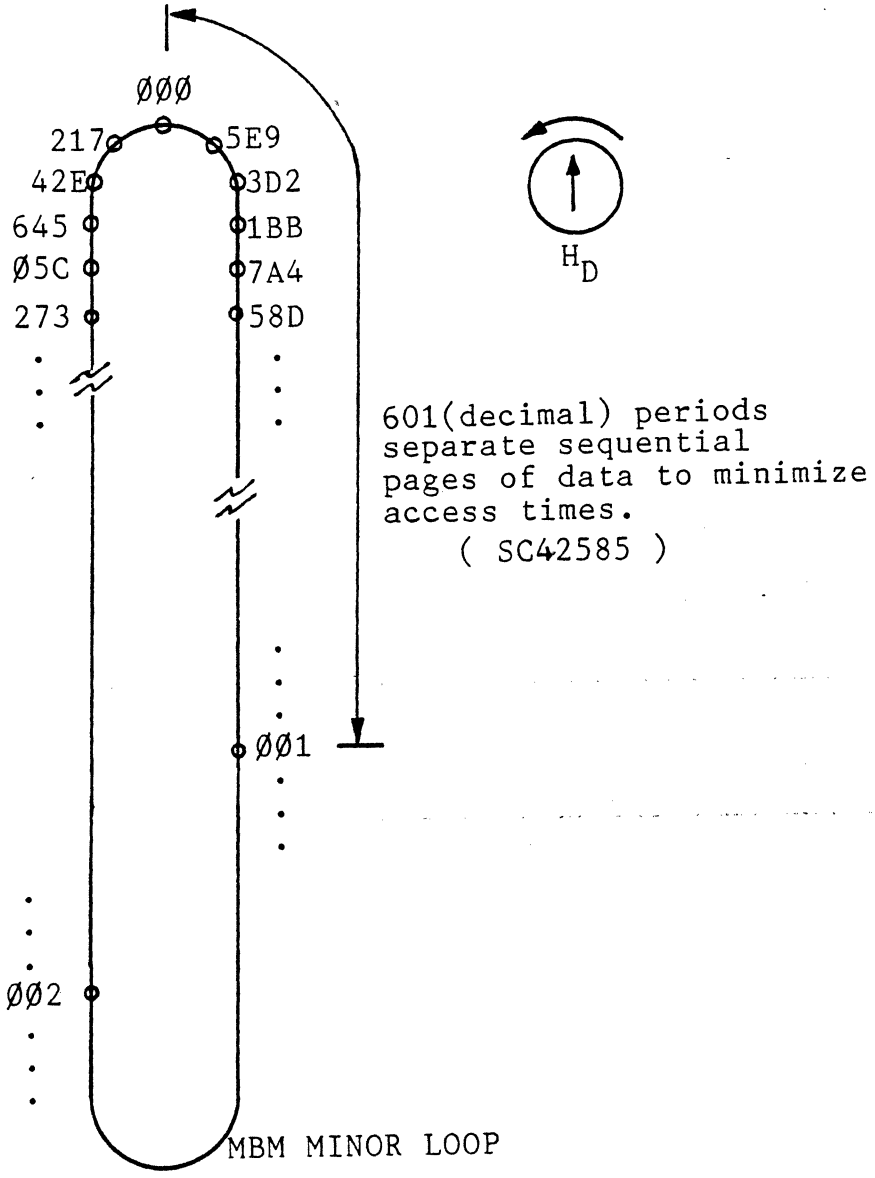


FIGURE 3.22

MBM ADDRESSING TECHNIQUE

The MBM controller acts as the timing master for the entire bubble memory subsystem. It must provide for an orderly start-up and shut-down of the coil driver circuitry so as to prevent the accidental loss of data in the bubble memory devices. It does so by way of four coil timing signals (i.e., XA, XB, YA, YB). These signals are sent to the coil predriver support circuits where they are level-shifted and converted to eight control lines. When a power failure is sensed (by the coil predriver, operation driver or user system) and RESET/ is activated, the controller ensures an orderly shut-down of the coil currents within three MBM propagation cycles. The worst case condition is that in which the swap operation has already begun, in which case the controller completes the swap and then orderly shuts down. Either way, the old data or new data is maintained rather than losing both pages.

As mentioned earlier, the MBM controller monitors the page of data with respect to the replicate and swap gates. It therefore issues, at the proper time, the operation driver control signals to swap, replicate, and generate data. In the case of reading data, it also informs the sense amplifier as to the time in a propagation cycle at which bubble domains are crossing the active detector. Figure 3.23 is a timing diagram for the MBM controller output signals.

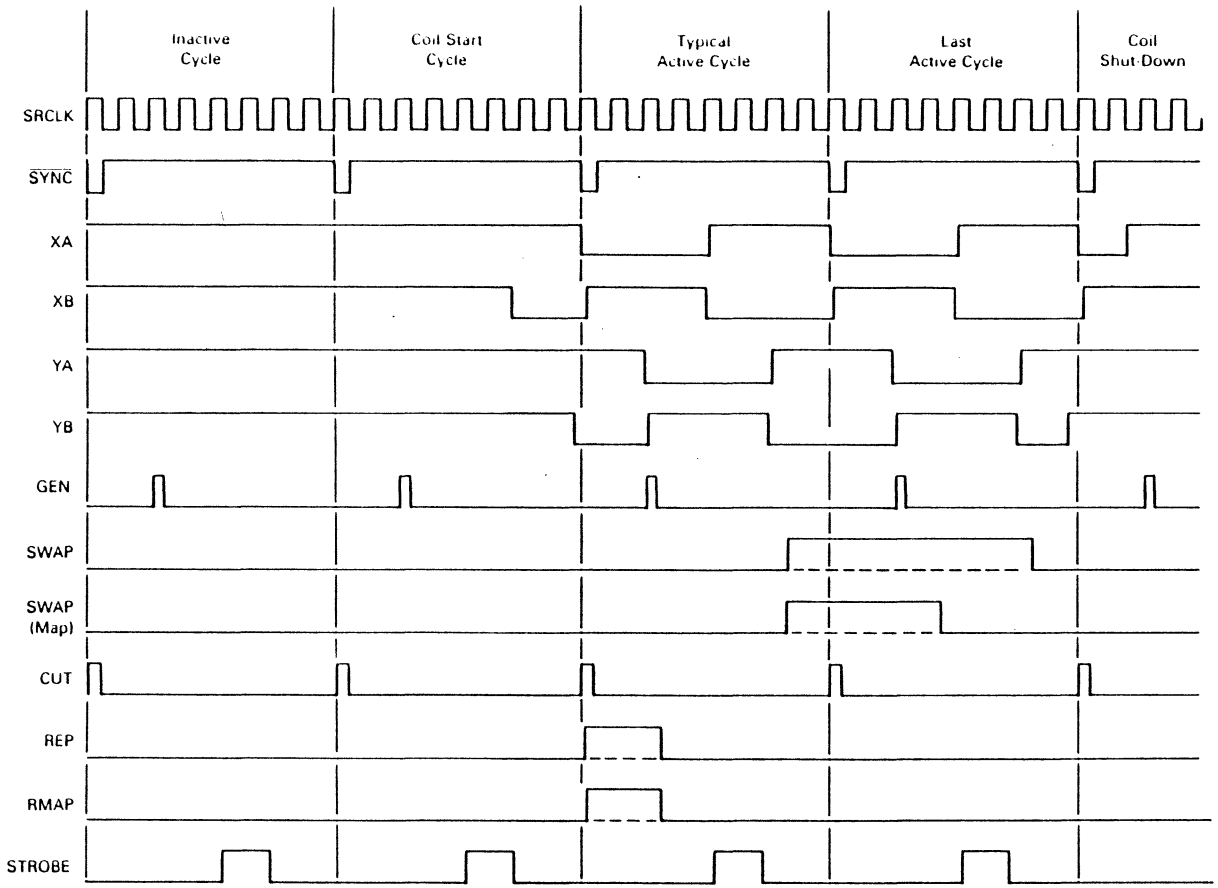


FIGURE 3.23

MBM CONTROLLER SUBSYSTEM TIMING

Additional control signals are provided for multiple-device bubble memory systems. These signals are used to clock data to/from the parallel subsystem from/into the controller serial data output/input lines at eight times the data rate of a one-device system. This subject is discussed in Chapter 4. Since the internal controller MAP RAM is only large enough for the RMPI of one-device (or two MBM2256s), control signals are provided to expand this memory capacity using external RAM or PROM.

3.2.4 Error Detection and Correction

The MBM controller contains error detection and correction logic to increase overall bubble memory system reliability. Error mechanisms observed in bubble memories differ vastly from those encountered in semiconductor memories.

As in conventional semiconductor memories, errors in an MBM subsystem can be classified into two general categories: hard or soft errors. Hard errors are errors that are the result of data inversion within a minor loop. Subsequent reads to the page in error will always result in the same error being detected. Unlike hard errors in semiconductor memories, though, the page of data can be rewritten in the bubble memory. A soft error, in contrast, usually results from mishaps or transient voltages in the actual detection operation of the bubble memory read.

Subsequent reads to the page in error almost always result in the correct reading of the page of data previously in error. With the relatively small magnitude of detector differential output signals, a noise spike from the system power supply could affect the detection of a single bit or burst of bits. (Since data are read serially.)

In addition to detection errors, the error mechanisms observed in bubble memories (usually the result of operating the memory outside the specified operating region) include bubble collapse, bubble stripout, spontaneous nucleation, or bubble slip. A bubble collapsing on the read track results in a single-bit soft error. The original data stored in the minor loops is unaffected. Bubble collapse in the minor loop or on the write track before the swap operation will result in a single-bit hard error.

Bubble stripout (a bubble domain splits in two) on the read track will most probably result in a single-bit soft error. On the write track or in a minor loop, a single-bit hard error may result.

Bubble nucleation is usually the result of a film defect. In this case, spurious bubbles are emitted from the defect and can produce multiple hard errors. However, the block structure of the memory makes the nucleation within minor loops usually affect only one-bit per page of data.

A bubble slip results from a bubble domain failing to propagate to the next memory cell. On the read track this can result in a double-bit soft error. Bubble slip in the minor loop results in two hard errors, but in two separate pages (i.e., two separate ECC blocks), again because of the block structure of the memory. Finally, a bubble slip on the write track can result in a double-bit hard error.

As described above, the most predominant errors in bubble memories, although infrequent, tend to occur as single-bit or small bursts of errors. To handle these potential error occurrences, the MBM controller contains error detection and correction circuitry designed to correct all single-bit errors and all bursts of errors up to and including three bits. In addition, the controller will detect all errors up through a 12-bit burst. A very small portion of errors in excess of 12-bit bursts may go undetected.

The ECC bits are generated by the controller and appended onto the end of every 512-bit data block during write operations, forming a 524-bit ECC block. During read commands, the ECC circuitry checks the ECC block and sets the appropriate error flags if an error is detected.

The error with the highest probability of occurrence is a transient or soft-read error in the sensing channel.

The best approach to processing an error occurrence is, therefore, to reread the page in error. If the error appears again, it can be assumed that the error is hard and the READ CORRECTED command can then be executed to correct the error. The page should thereafter be rewritten with the corrected data.

The MBM controller uses a 12-bit Fire code to implement the error detection and correction operation. The error detection and correction capability of this code is summarized in Table 3.4. The generator polynomial is:

$$g(X) = X^{12} + X^{11} + X^{10} + X^9 + X^4 + X^2 + X + 1$$

In factored irreducible polynomial form:

$$g(X) = (X^{2b-1} + 1)\ p(X)\ ,$$

where b = burst error correcting capability

p(X) = irreducible polynomial.

$$g(X) = (X^5 + 1)\ (X^7 + X^6 + X^5 + X^4 + X^2 + X + 1)$$

Thus, the Fire code selected is shown to have a burst error correction capability of 3 or less bit bursts.

The ECC encoder for this generator polynomial is shown in Figure 3.24. During the execution of a WRITE DATA or WRITE MAP LOOP command, the controller appends twelve ECC bits onto the end of every 512-bit data block. This forms

FIRE CODE PERFORMANCE

ERROR PATTERN	DETECTION	CORRECTION
1 Random bit	100%	100%
2 Random bits	100%	0%
3 Random bits	100%	0%
>3 Random bits	>99%	0%
1-3 bit Burst	100%	100%
4-12 bit Burst	100%	0%
>12 bit Burst	>99%	0%

TABLE 3.4

FIRE CODE PERFORMANCE

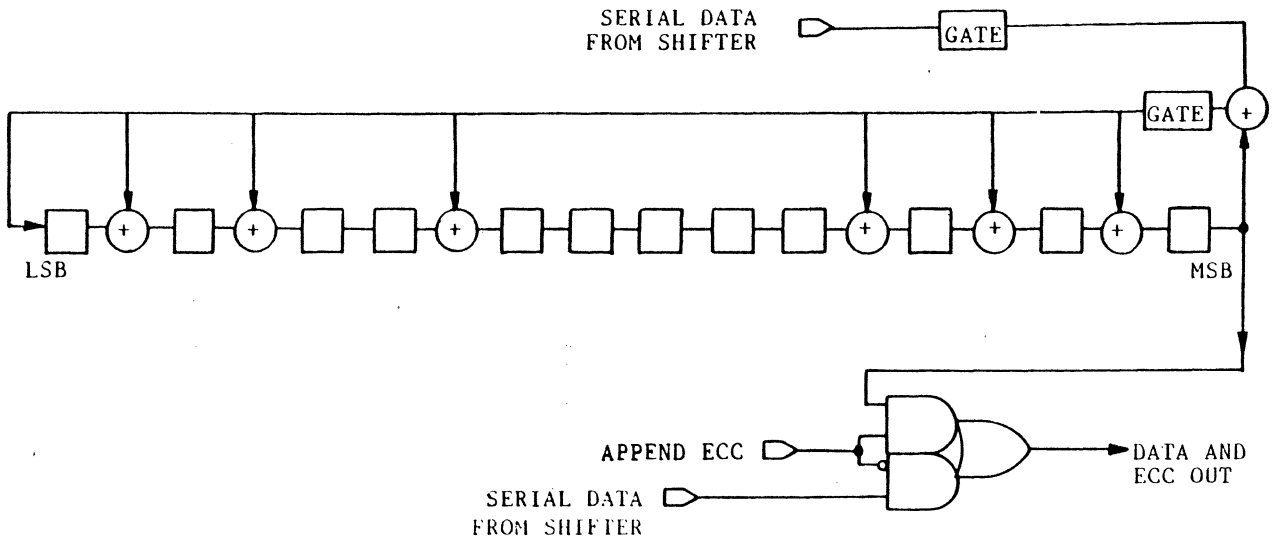


FIGURE 3.24

MBM CONTROLLER ECC ENCODER

the 524-bit ECC block that is then sent to the output mapper stage, where the redundant loop management function is applied.

The ECC decoder is shown in Figure 3.25. In addition to the logic of the ECC encoder, the ECC decoder contains an error-trapping scheme along with the error correction logic. During the execution of an INITIALIZE, READ DATA or READ MAP LOOP command, the ECC decoder turns on gates A and B, calculates the syndrome bits, and flags an error if they are not all zeroes. In this case, the syndrome bits are then stored in a syndrome latch. The execution of a READ CORRECTED command immediately following the detection of the page in error, then acts to circulate the data in the decoder while the reread data is being shifted in from the bubble memory subsystem. In this case, gates A and C are turned off and gates B and D are turned on. Once the error is trapped, (i.e., the nine highest order decoder bits are all zero), the error pattern is contained in the low-order three decoder bits. At this time, gate B is turned off and gate C is turned on. Within the next three shifts of data, errors will be corrected.

To prevent the occurrence of two different errors occurring during the first read and corrected read operations, the ECC encoder is also activated to calculate the syndrome bits on the incoming data bits of the READ CORRECTED

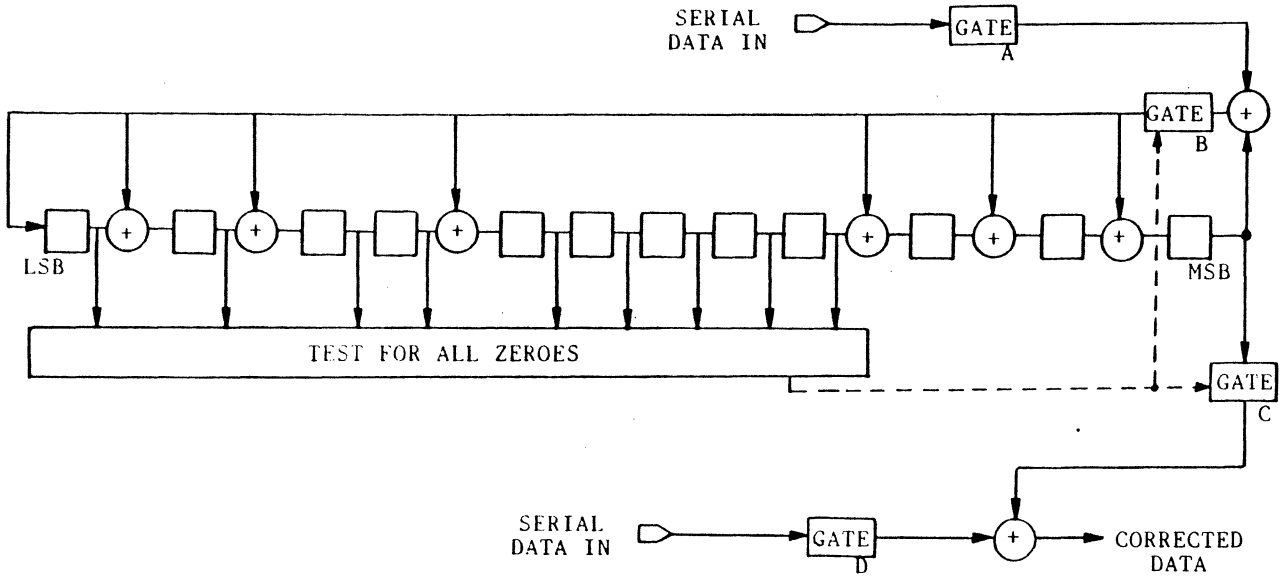


FIGURE 3.25

MBM CONTROLLER ECC DECODER AND ERROR TRAPPING LOGIC

operation. Following the READ CORRECTED command execution, the encoder-calculated syndrome bits are then compared with that stored by the decoder from the original data read. See Figure 3.26. If the two syndromes do not match, an error indication is generated signifying that a soft error was present.

Let p_e be the probability of a bit in error. Then, since the ECC block is 524 bits (512 data bits plus 12 ECC bits), the probability of no errors in an ECC block of data is:

$$P_0 = (1 - p_e)^{524}$$

For very small p_e, this value approaches one.

Assuming a binomial probability distribution, the probability of any number, n, of errors in the ECC block can then be expressed as:

$$P_n = C_n^{524} \, p_e^n \, (1 - p_e)^{524 - n}$$

And the probability of n-bit error occurrences in an ECC block for n = 1, 2, 3, 4 is given by:

$$P_1 = C_1^{524} \, p_e^1 \, (1 - p_e)^{523} \cong 524 \, p_e$$

$$P_2 = C_2^{524} \, p_e^2 \, (1 - p_e)^{522} \cong (1.37 \times 10^5) \, p_e^2$$

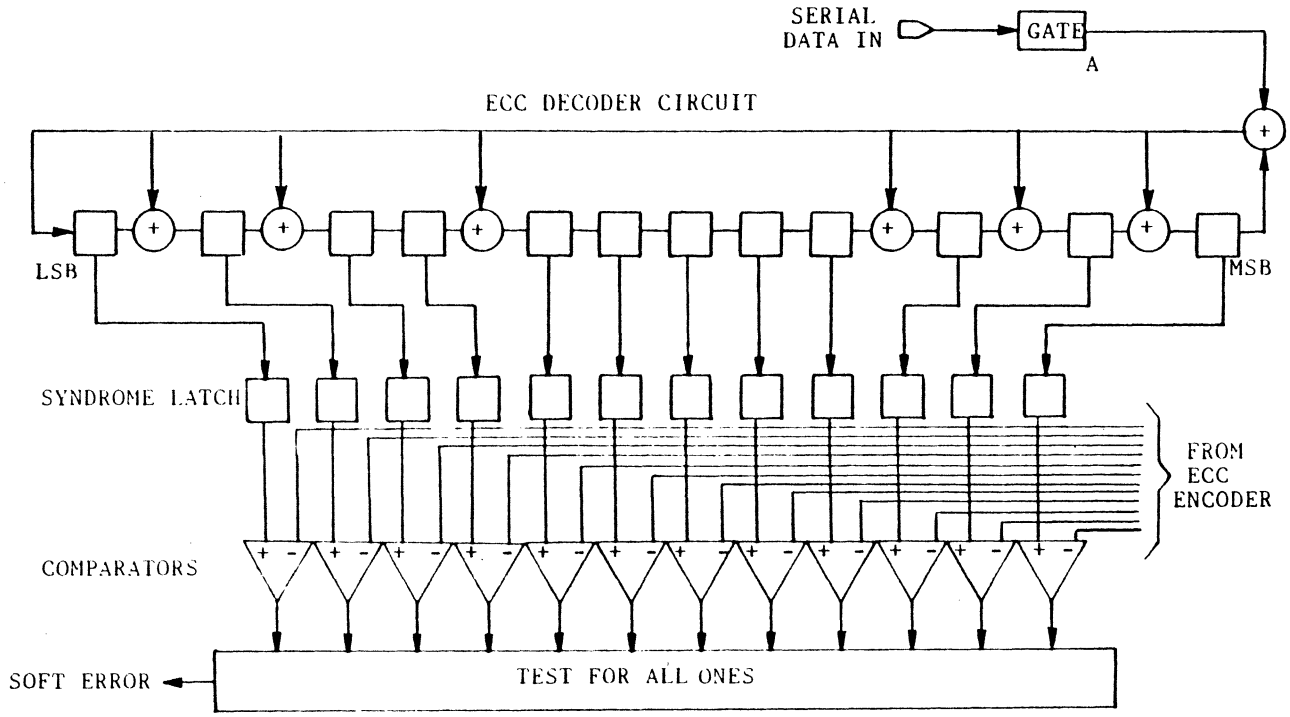


FIGURE 3.26

MBM CONTROLLER SOFT ERROR DETERMINATION

$$P_3 = C_3^{524}\, p_e^3\, (1 - p_e)^{521} \cong (2.38 \times 10^7)\, p_e^3$$

$$P_4 = C_4^{524}\, p_e^4\, (1 - p_e)^{520} \cong (3.11 \times 10^9)\, p_e^4$$

Since P_1 is very much larger than $\sum_{n=2}^{524} P_n$ for small p_e, the the probability of any error occurrence is approximately P_1. Using the error correction capability improves overall system performance by decreasing the probability of error to approximately P_2. (Although the ECC logic corrects for 1 to 3-bit bursts, it will not correct a 2-bit random error.) Table 3.5 shows the improvement in system performance based on error-free operation for various raw bit error rates (BERR), p_e.

Figure 3.27 is a die photograph of the MBM controller.

3.3 THE COIL PREDRIVER/DRIVER

The SC42468 Bubble Memory Coil Predriver is a 20-pin CMOS monolithic integrated circuit designed to convert the TTL-compatible coil timing signals of the MBM controller into level-shifted control signals required by the MTQ5NP03 complementary MOS transistor bridge. The MBM controller, MBM Coil Predriver and MOS transistor network work together to produce the triangular drive currents of the X and Y bubble memory coils.

P_e (BERR)	NO CORRECTION		WITH CORRECTION		
	BLOCK ERROR RATE ($\cong P_1$)	MEAN TIME BETWEEN ERRORS*	BLOCK ERROR RATE ($\cong P_2$)	EQUIVALENT BERR	MEAN TIME BETWEEN ERRORS*
10^{-8}	5×10^{-6}	19.1 min	1.4×10^{-11}	2.7×10^{-14}	13.5 yr
10^{-9}	5×10^{-7}	3.2 hr	1.4×10^{-13}	2.7×10^{-16}	1346 yr
10^{-10}	5×10^{-8}	31.9 hr	1.4×10^{-15}	2.7×10^{-18}	1.3×10^{5} yr
10^{-11}	5×10^{-9}	13.3 days	1.4×10^{-17}	2.7×10^{-20}	1.3×10^{7} yr
10^{-12}	5×10^{-10}	132.7 days	1.4×10^{-19}	2.7×10^{-22}	1.3×10^{9} yr
10^{-13}	5×10^{-11}	3.6 yr	1.4×10^{-21}	2.7×10^{-24}	1.3×10^{11} yr

*Time calculated based on maximum transfer rate of single one megabit system.

TABLE 3.5

EFFECTS OF CORRECTION ON PERFORMANCE

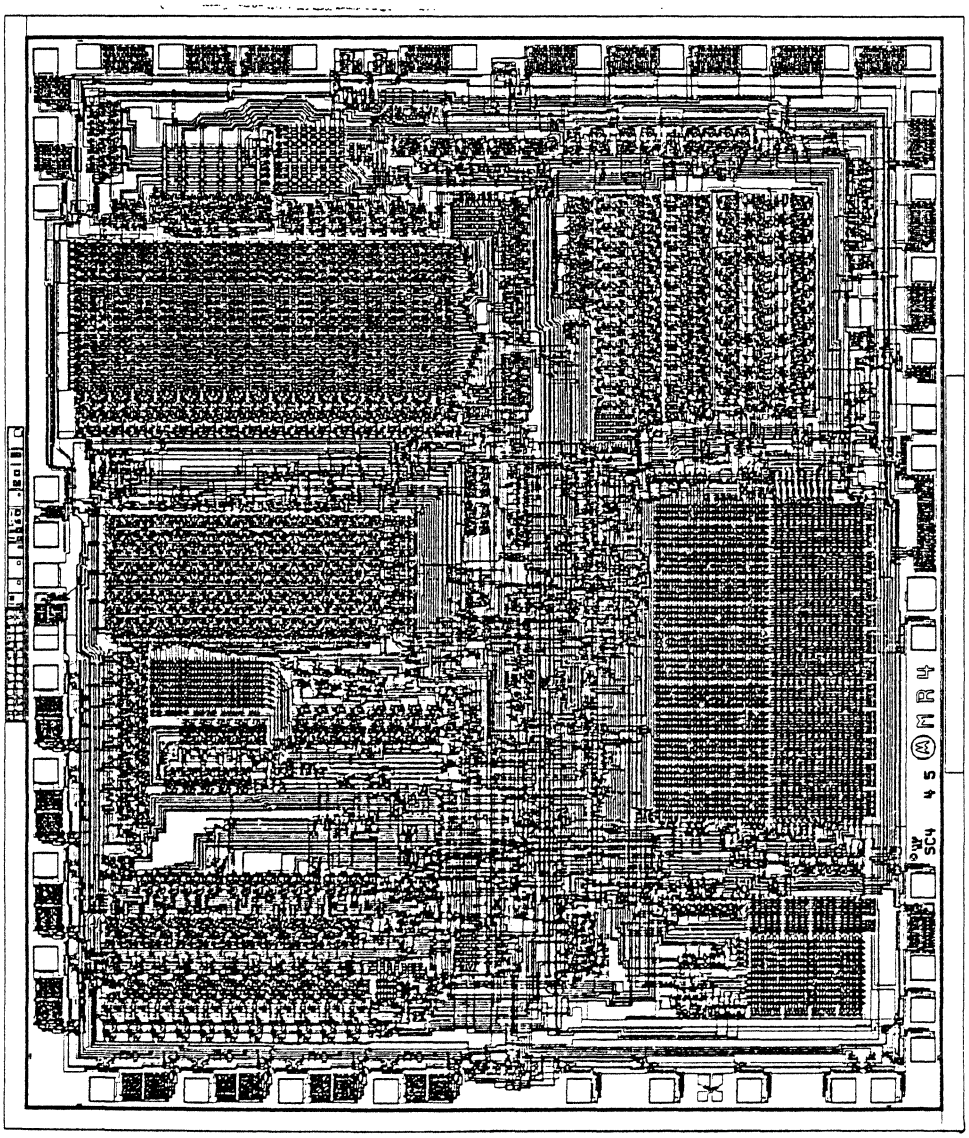


FIGURE 3.27

MBM CONTROLLER DIE PHOTOGRAPH

In addition, the MBM Coil Predriver has an internal voltage sensing circuit designed to inform the controller when supply voltages (+5V and +12V) are not within the specified region. In this way, the controller can then perform an orderly shut-down of its operation and prevent the accidental loss of data. An interlock signal, RUN, is also provided as a feature and is designed to enable other support circuits only when the bubble memory coils are activated, thereby disabling any accidental current functions from distrubing the stored data. A chip select is provided for implementing multiplexed, multiple-MBM systems. Figure 3.28 is a logic diagram for the SC42468 MBM Coil Predriver.

The MBM Coil Predriver converts the two (two for each coil) MBM controller timing signals for activating the coil driver network to four 0-to-10 volt control signals which act to switch on alternate pairs of the P- and N-channel power FETs. The power FETs and MBM coils are configured in a bridge network as illustrated in Figure 3.29.

In the off-state, the MBM controller signals XA, XB, YA and, YA are all in the high state and, subsequently, the Coil Predriver outputs X+, $\overline{X+}$, Y+, $\overline{Y+}$ are also in the high-state (10 volts). This keeps the two N-channel FETs turned on and effectively grounds both ends of the coils.

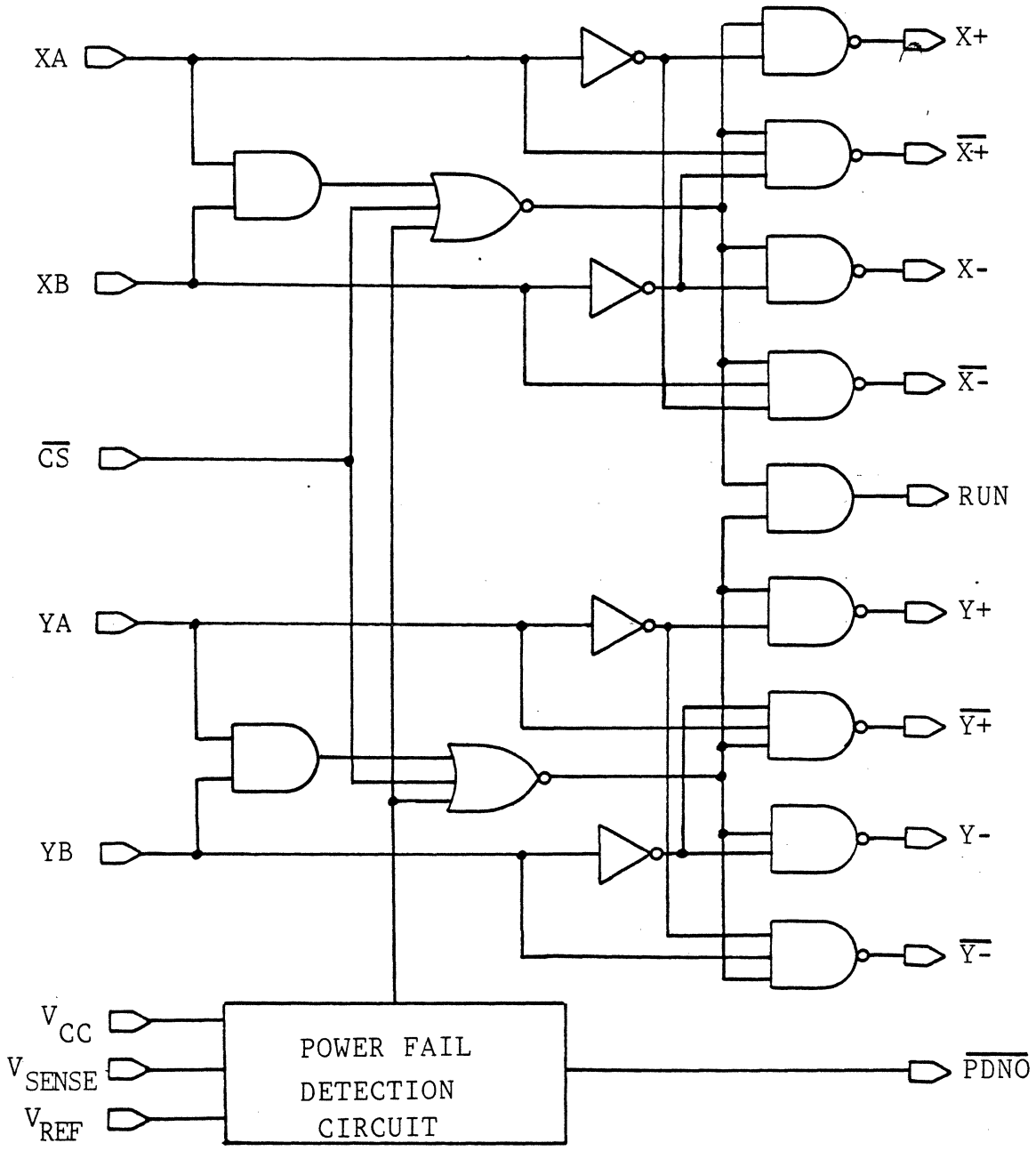
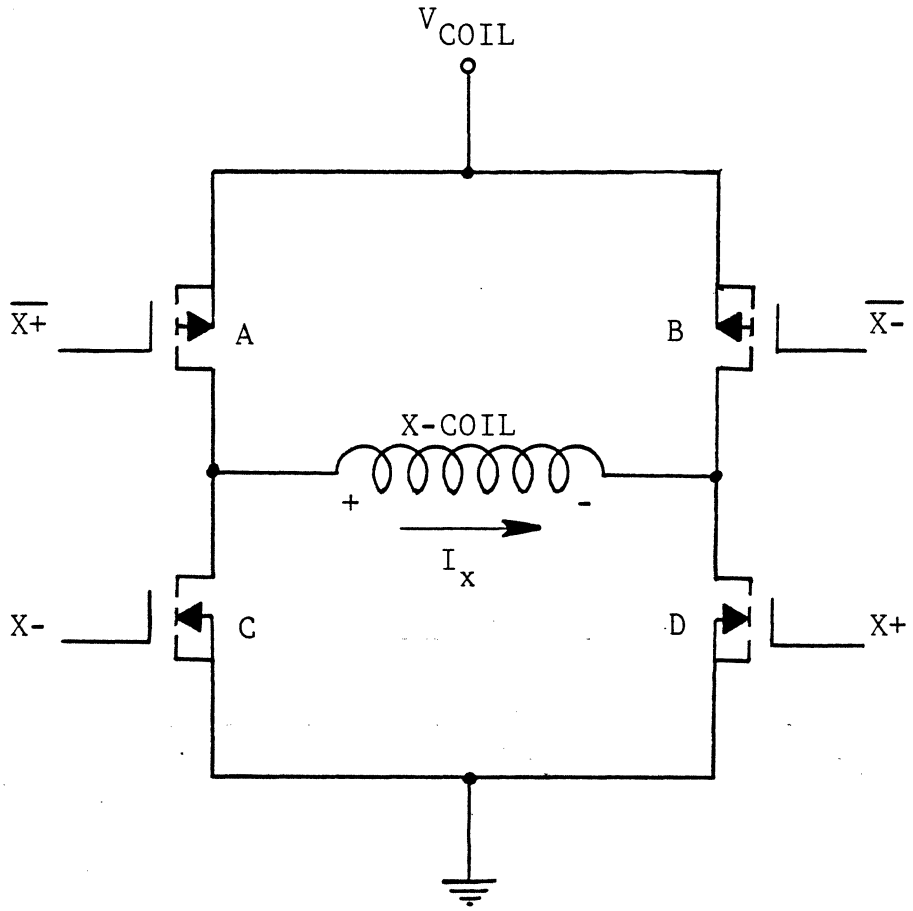


FIGURE 3.28

MBM COIL PREDRIVER LOGIC BLOCK DIAGRAM



NOTE: Corresponding connections are made for the Y-coil.

FIGURE 3.29

COIL DRIVER CONNECTIONS TO MBM COILS

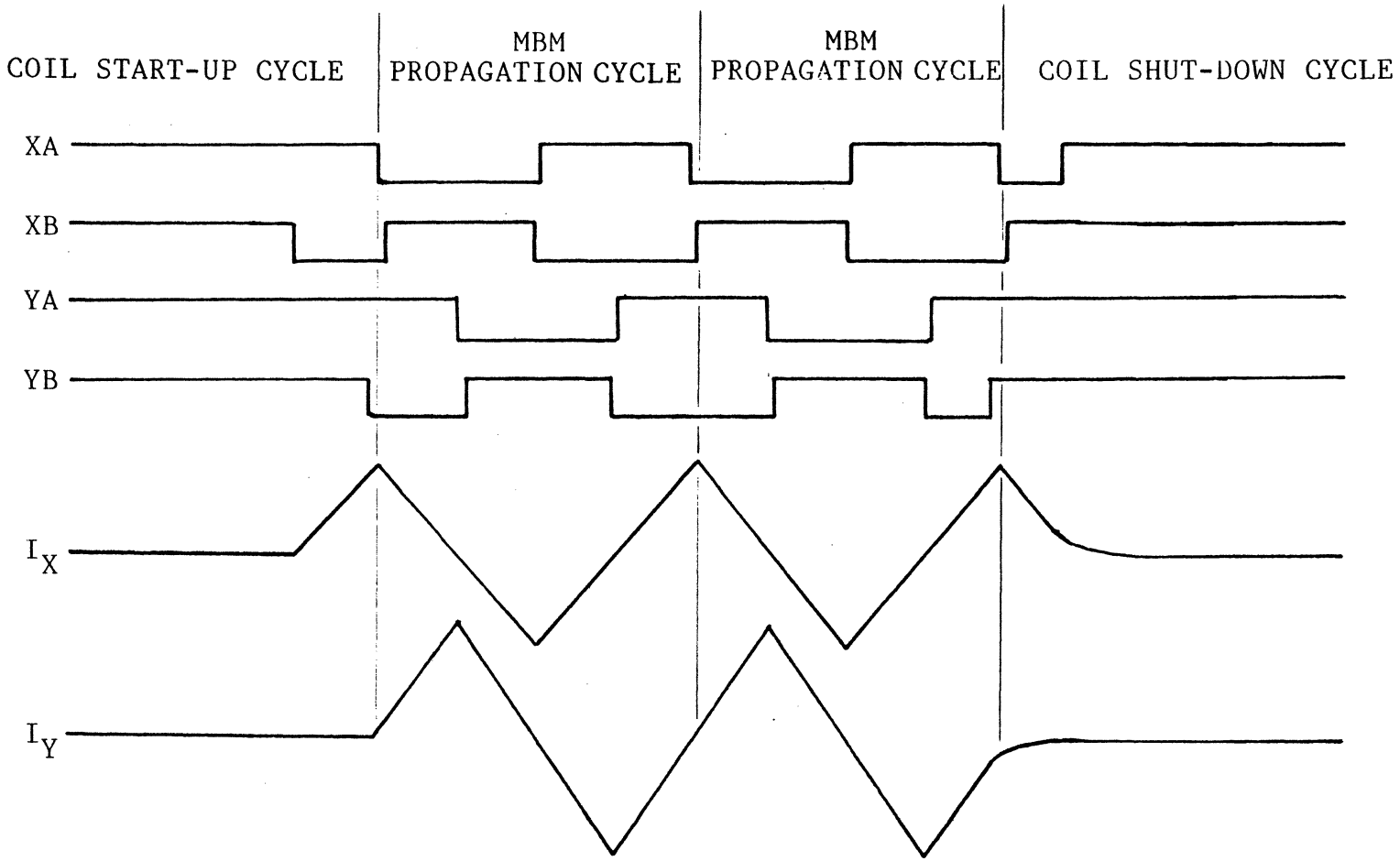


FIGURE 3.30

COIL CURRENT TIMING

To supply positive ramping current to the coils (making use of the resistive and inductive effects of the coil and FET on-resistance), the FETs denoted B and C in Figure 3.29 are turned off and FETs A and D are turned on. This results in V_{coil} being instantaneously supplied across the RL circuit and a ramping current results. In the same manner, negative coil current is supplied through the coil when FETs A and D are turned off followed by FETs B and C being turned on.

During the coil shut-down cycle, the coil currents are ramped to near zero, but before they reach zero current, are allowed to exponentially decay as both ends of the coil are once again grounded. See Figure 3.30.

To calculate peak X and Y coil currents, consider the model circuit given in Figure 3.31. At time t=0, when the P- and N-channel pair of power FETs are switched on, V_{coil} appears across the coil inductance (L_c) and resistance (R_c) and the on-resistances of the FETs (Ronp and Ronn).

Summing the voltage drops around the model circuit results in:

$$V_{coil} = L_c \frac{di_c}{dt} + i_c R_c + i_c R_{onp} + i_c R_{onn}$$

$$V_{coil} = L_c \frac{di_c}{dt} + i_c(R_c + R_{omp} + R_{onn}) \quad (3.3.1)$$

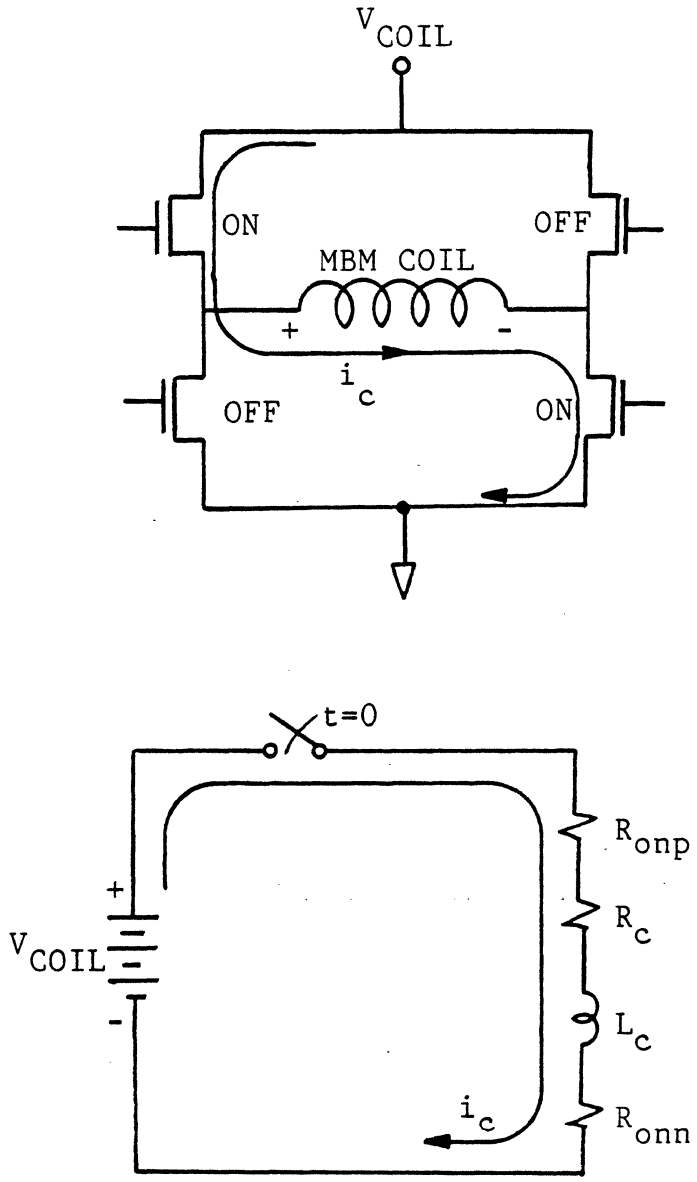


FIGURE 3.31

COIL DRIVER MODEL CIRCUIT

Dividing by L_c gives:

$$\frac{V_{coil}}{L_c} = \frac{di_c}{dt} + \frac{i_c(R_c + R_{onp} + R_{onn})}{L_c}$$

Let $R_t = (R_c + R_{onp} + R_{onn})$, then

$$\frac{V_{coil}}{L_c} = \frac{di_c}{dt} + \frac{i_c R_t}{L_c} \qquad (3.3.2)$$

Now using an integrating factor, let $\emptyset$ be a function such that:

$$\emptyset\frac{di_c}{dt} + \frac{R_t}{L_c}\emptyset i_c = \frac{d}{dt}(\emptyset i_c) \qquad (3.3.3)$$

$$\emptyset\frac{di_c}{dt} + \frac{R_t}{L_c}\emptyset i_c = \emptyset\frac{di_c}{dt} + i_c\frac{d\emptyset}{dt}$$

Subtracting $\emptyset\frac{di_c}{dt}$:

$$\frac{R_t}{L_c}\emptyset\, i_c = i_c\frac{d\emptyset_c}{dt}$$

Dividing by i_c to obtain:

$$\frac{R_t}{L_c}\emptyset = \frac{d\emptyset}{dt}$$

Now solve by using separation of variables:

$$\frac{d\emptyset}{\emptyset} = \frac{R_t}{L_c}\, dt$$

$$\int \frac{d\emptyset}{\emptyset} = \frac{R_t}{L_c} \int dt$$

$$\ln\emptyset = \frac{R_t}{L_c}\, t$$

$$\emptyset = e^{\frac{R_t}{L_c} t} \qquad (3.3.4)$$

Thus, $\emptyset$ is the intehrating factor and the following equation results when the integrating factor is multiplied by equation (3.3.2):

$$\frac{V_{COIL}}{L_c}\, e^{\frac{R_t}{L_c}t} = e^{\frac{R_t}{L_c}t} \frac{di_c}{dt} + e^{\frac{R_t}{L_c}t} \frac{R_t}{L_c} i_c$$

Using equation (3.3.3):

$$\frac{d}{dt}\left(e^{\frac{R_t}{L_c}t}\, i_c\right) = \frac{V_{COIL}}{L_c}\, e^{\frac{R_t}{L_c}t} \qquad (3.3.5)$$

Integrating both sides of equation (3.3.5) gives:

$$\int \frac{d}{dt}\left(e^{\frac{R_t}{L_c}t}\, i_c\right) dt = \frac{V_{COIL}}{L_c} \int e^{\frac{R_t}{L_c}t}\, dt + C$$

where C is the constant of integration. Evaluating,

$$e^{\frac{R_t}{L_c}t}\, i_c = \frac{V_{COIL}}{L_c}\left(\frac{L_c}{R_t}\right) e^{\frac{R_t}{L_c}t} + C$$

Multiplication by $e^{\frac{-R_t}{L_c}t}$ results in:

$$i_c = \frac{V_{COIL}}{R_t} + Ce^{\frac{-R_t}{L_c}t}$$

To evaluate the constant of integration, C, the initial conditions are applied:

$$\left.\begin{array}{r} t = 0 \\ i_c(0) = 0 \end{array}\right\} \Rightarrow C = \frac{-V_{COIL}}{R_t}$$

The final solution, therefore, is:

$$i_c(t) = \frac{V_{COIL}}{R_t} - \frac{V_{COIL}}{R_t} e^{\frac{-R_t}{L_c}t}$$

or,

$$i_c(t) = \frac{V_{COIL}}{R_t} (1 - e^{\frac{-R_t}{L_c}t}) \qquad (3.3.7)$$

From equation (3.3.7), it is seen that the coil current is exponential, rather than a true ramp. However, if the on-time of the FETs is much less than the time constant of the RL circuit, then the coil currents will appear to ramp.

A die photograph of the SC42468 MBM Coil Predriver is given in Figure 3.32.

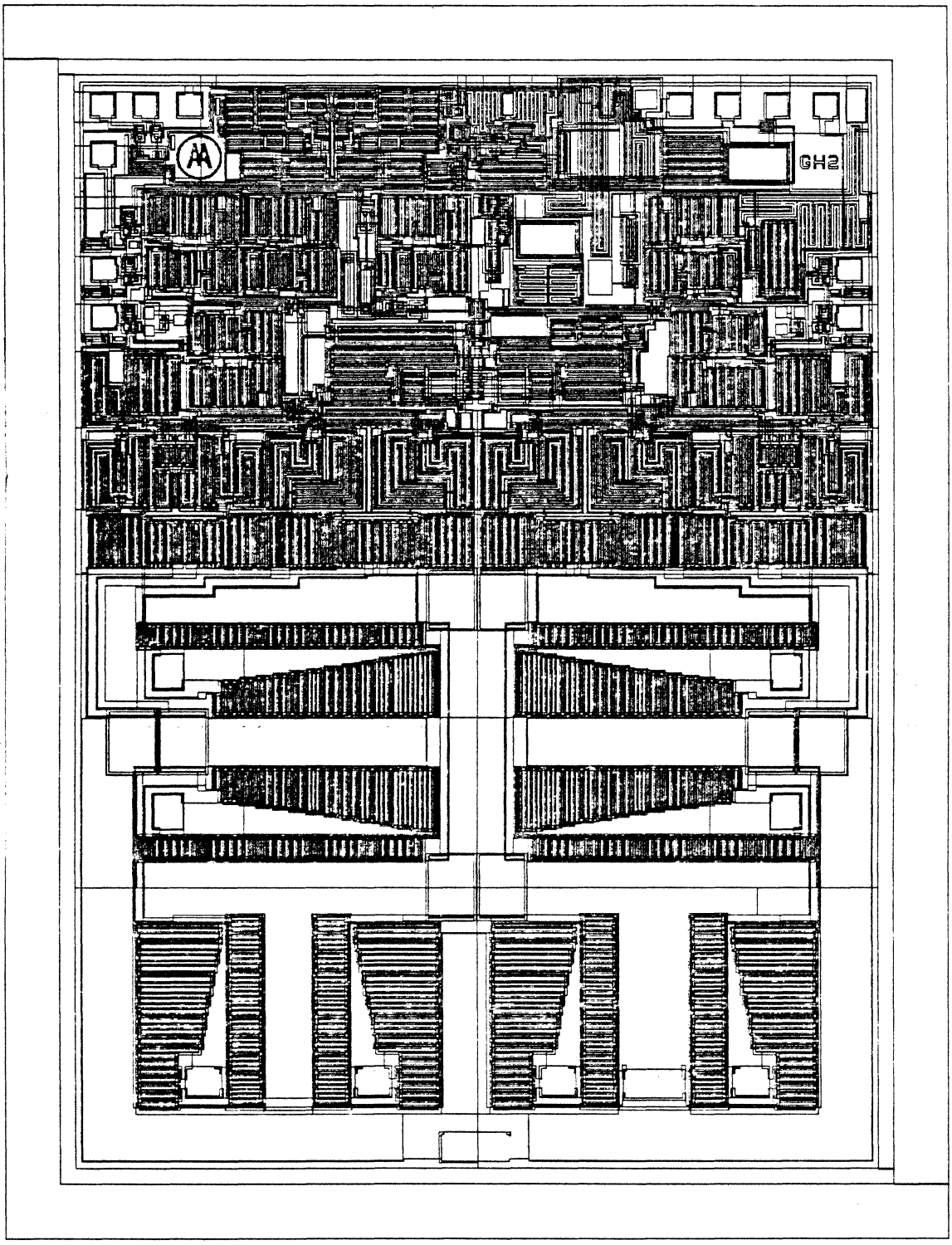


FIGURE 3.32

MBM COIL PREDRIVER DIE PHOTOGRAPH

3.4 THE DUAL MBM OPERATION DRIVER

The MC34046 and MC34047 Dual Bubble Memory Operation Drivers are bipolar linear monolithic integrated circuits designed for use with Motorola's MBM2256 and MBM2011 bubble memory devices, respectively. They are contained in 28-pin dual-in-line packages and are pin-compatible. Each MBM Operation Driver is capable of driving one or two bubble memory devices and requires only a single +5V supply. They differ only in operation current (also known as function current) amplitudes as required by the respective bubble memory devices they service.

The MBM Operation Driver features controlled-current sinks including controlled rise and fall times for performing the bubble memory read and write operations. In addition, the input pulse time-out circuitry prevents accidental damage to the bubble memory functional elements. Four pins are made available to individually set the function current amplitudes using precision resistors. In extended temperature environments, the function currents can be made to track the device temperature by using inexpensive resistor-thermistor networks. A chip select pin is provided for use as an interlock with the RUN signal of the MBM Coil Predriver.

The MBM Operation Driver also provides the high voltage required for the data swap and data replicate operations

as well as sensing circuitry to inform the MBM controller as to when the boost voltage has fallen out of the specified region. A logic block diagram of the MBM Dual Operation Driver is shown in Figure 3.33.

Each of the individual function currents (swap, generate, replicate and map replicate) must fulfill the unique requirements of the bubble memory device with regard to pulse width, amplitude, phase and current waveform shape. The MBM controller and MBM Operation Driver work together to ensure proper operation of the bubble memory device. The MBM controller outputs TTL-compatible voltage signals defining the phase, pulse width, and alignment timing requirements. The MBM Operation Driver, in turn, converts these voltage signals to precision controlled-current pulses with controlled rise and fall times and peak amplitudes selected by the set resistors. Figure 3.34 and 3.35 are graphs showing the relationship of the function current amplitudes in relation to the corresponding set resistance. The MBM Operation Driver is designed to produce the nominal specified function current amplitude when the set resistance is 6.19 Kohm.

The MAP REPLICATE and DATA REPLICATE function currents have the same general waveshape requirements. Their amplitude, though, always differs by a factor of two. Thus, a common set resistor is used to establish the cut currents,

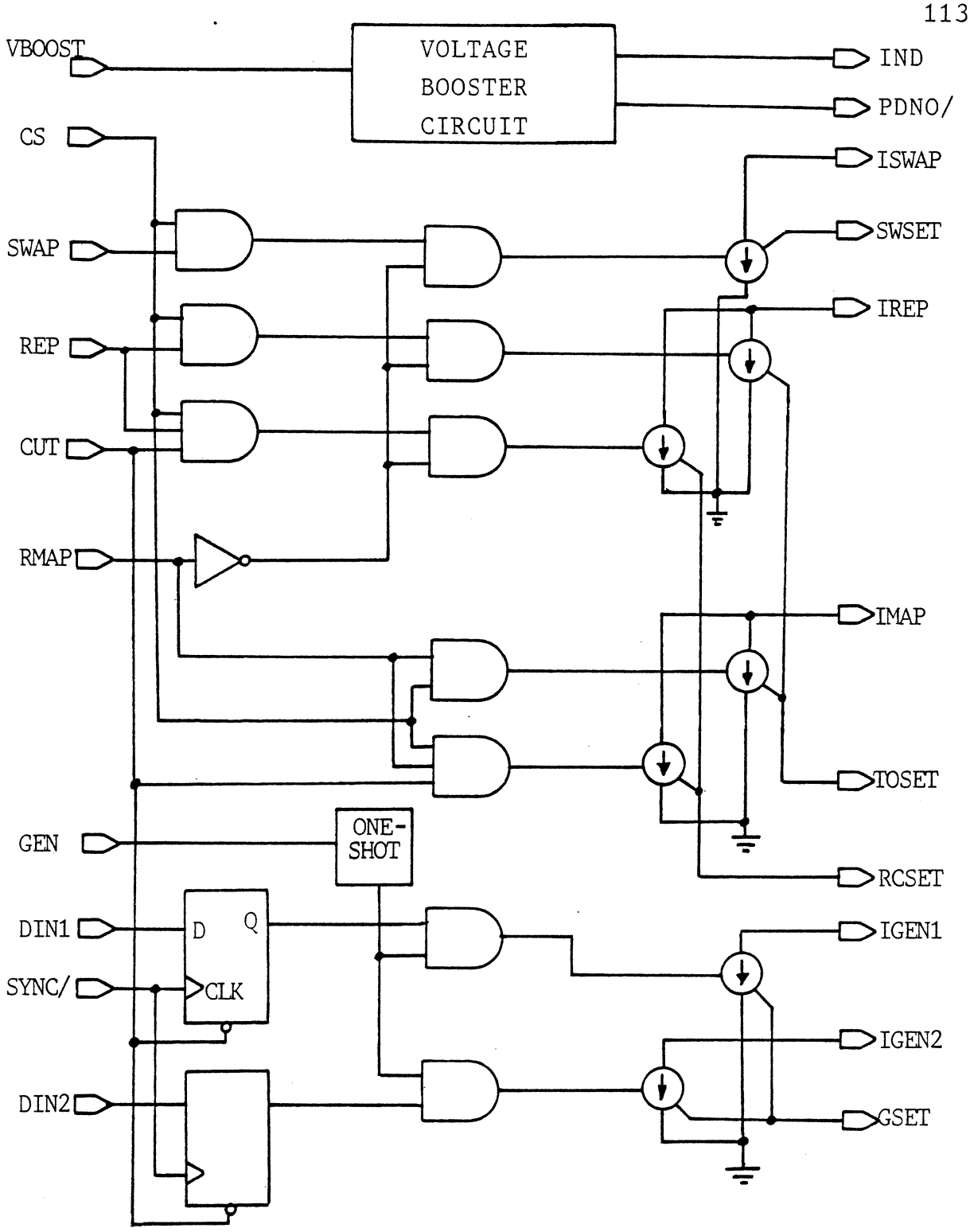


FIGURE 3.33

MBM OPERATION DRIVER LOGIC BLOCK DIAGRAM

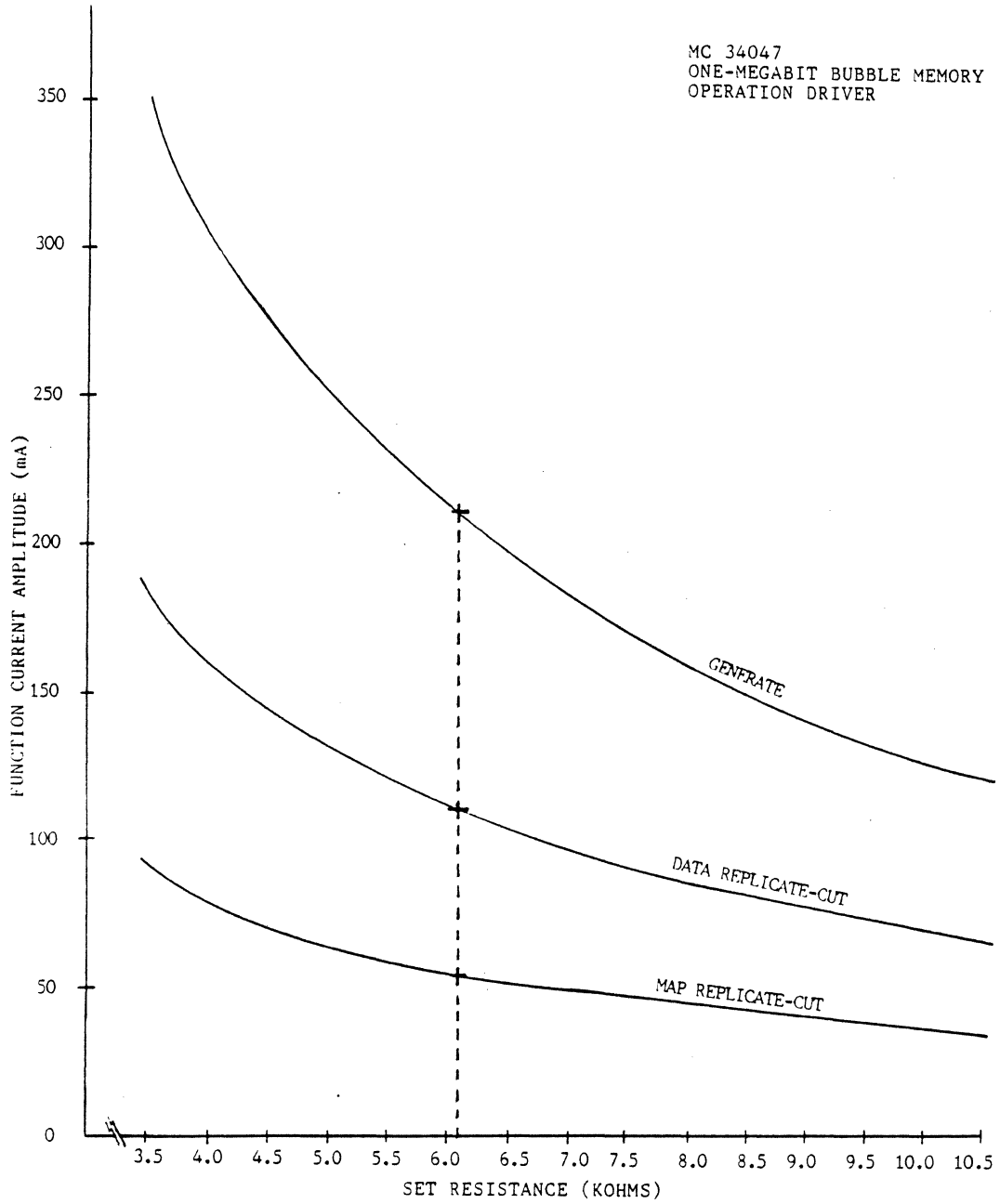


FIGURE 3.34

OPERATION DRIVER FUNCTION CURRENTS

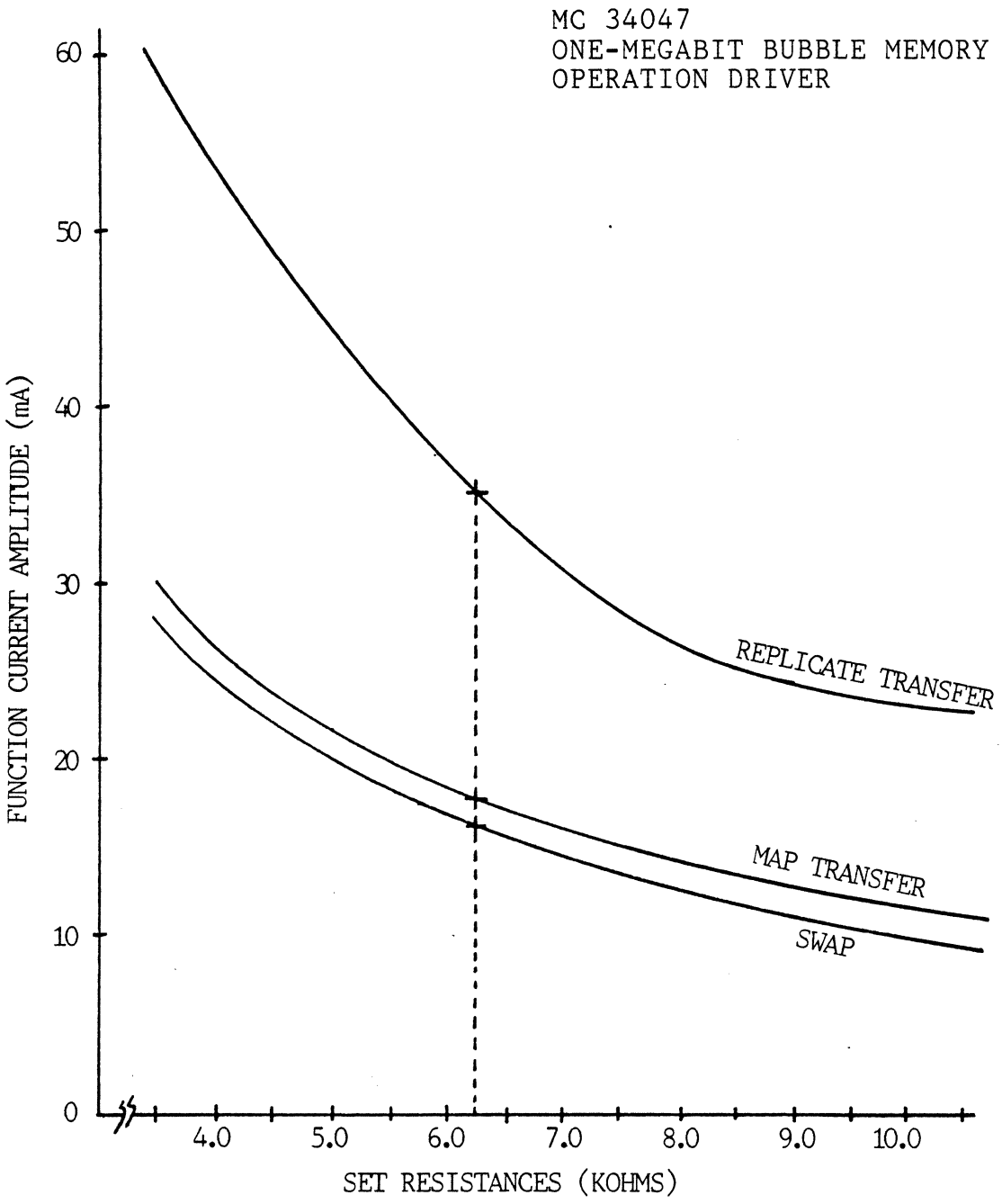


FIGURE 3.35

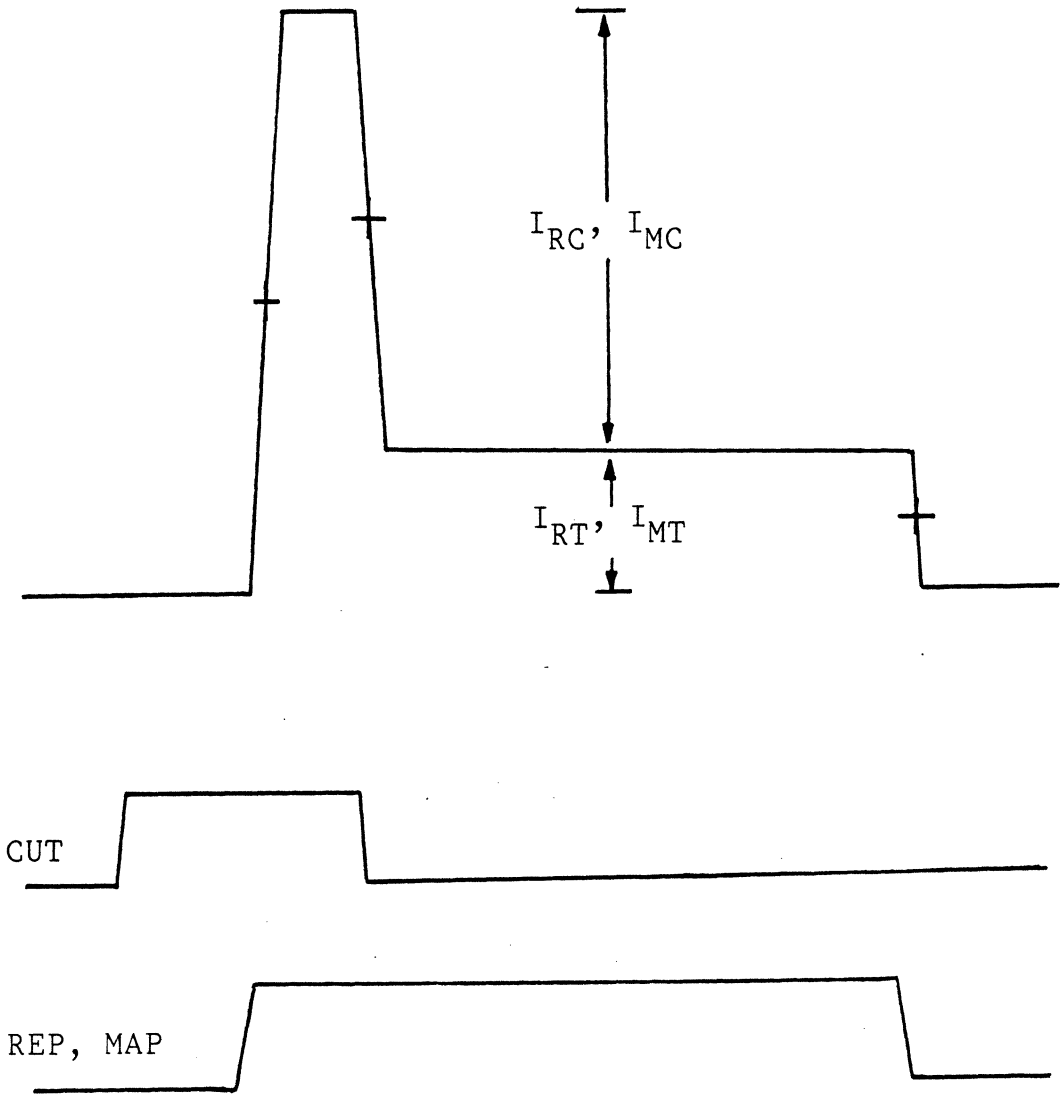
OPERATION DRIVER FUNCTION CURRENTS

I_{RC} and I_{MC}; another is used to establish the transfer-out currents, I_{RT} and I_{MT}. Note that the total established amplitude is the sum of the cut and transfer-out currents. See Figure 3.36. The CUT signal from the MBM controller is free-running, but the appropriate function current is output by the MBM Operation Driver only when the REP or MAP signal is concurrently received.

The generate function current, shown in Figure 3.37, is output when a serial data bit '1' is latched in by SYNC/ on DIN1 (or DIN2). GEN and SYNC/ are free-running, thus requiring that the write serial data line be high only when data are to be generated. A slow fall time is required by the MBM device to prevent the nucleation of multiple bubble domains.

The swap function current is shown in Figure 3.38. The resulting current is basically a DC low-level current established for approximately one full rotation of the drive field.

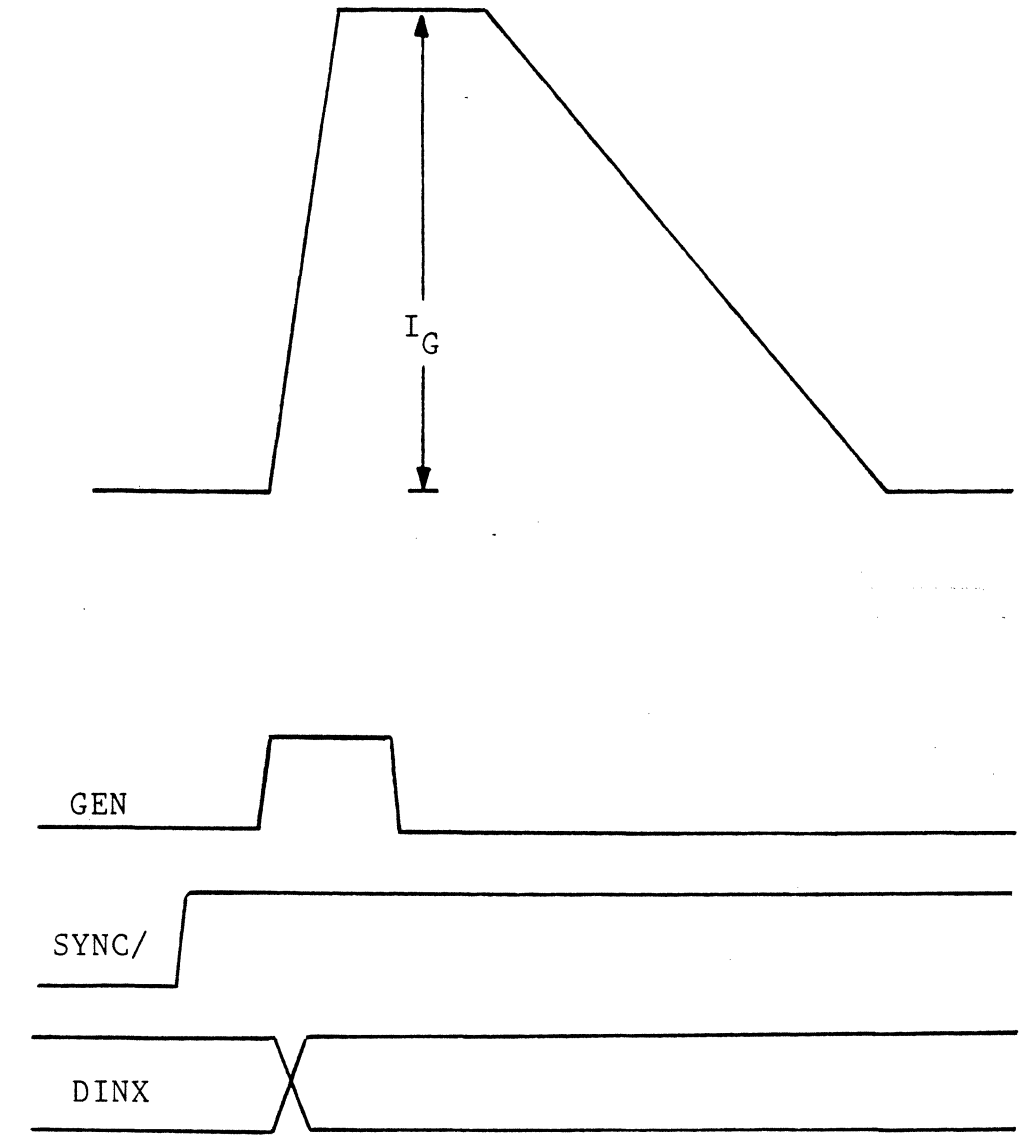
To supply the currents necessary for the high resistance swap and replicate gate elements, the MBM Operation Driver provides a booster voltage of 50 volts. An external storage capacitor, inductor, and diode are required as shown in Figure 3.39.



NOTE: CUT, REP, and MAP are signals generated by the MBM Controller.

FIGURE 3.36

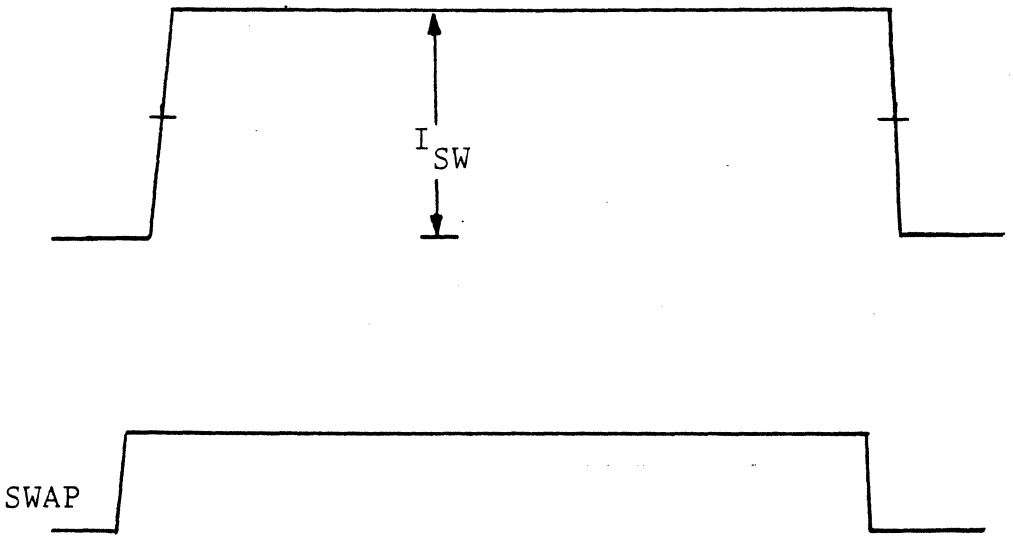
DATA AND MAP REPLICATE-CUT CURRENTS



NOTE: GEN, SYNC/, and DOUT (connected to DINX on the Operation Driver) are generated by the MBM Controller.

FIGURE 3.37

GENERATE FUNCTION CURRENT



NOTE: SWAP is a signal generated by the MBM Controller.

FIGURE 3.38

SWAP FUNCTION CURRENT

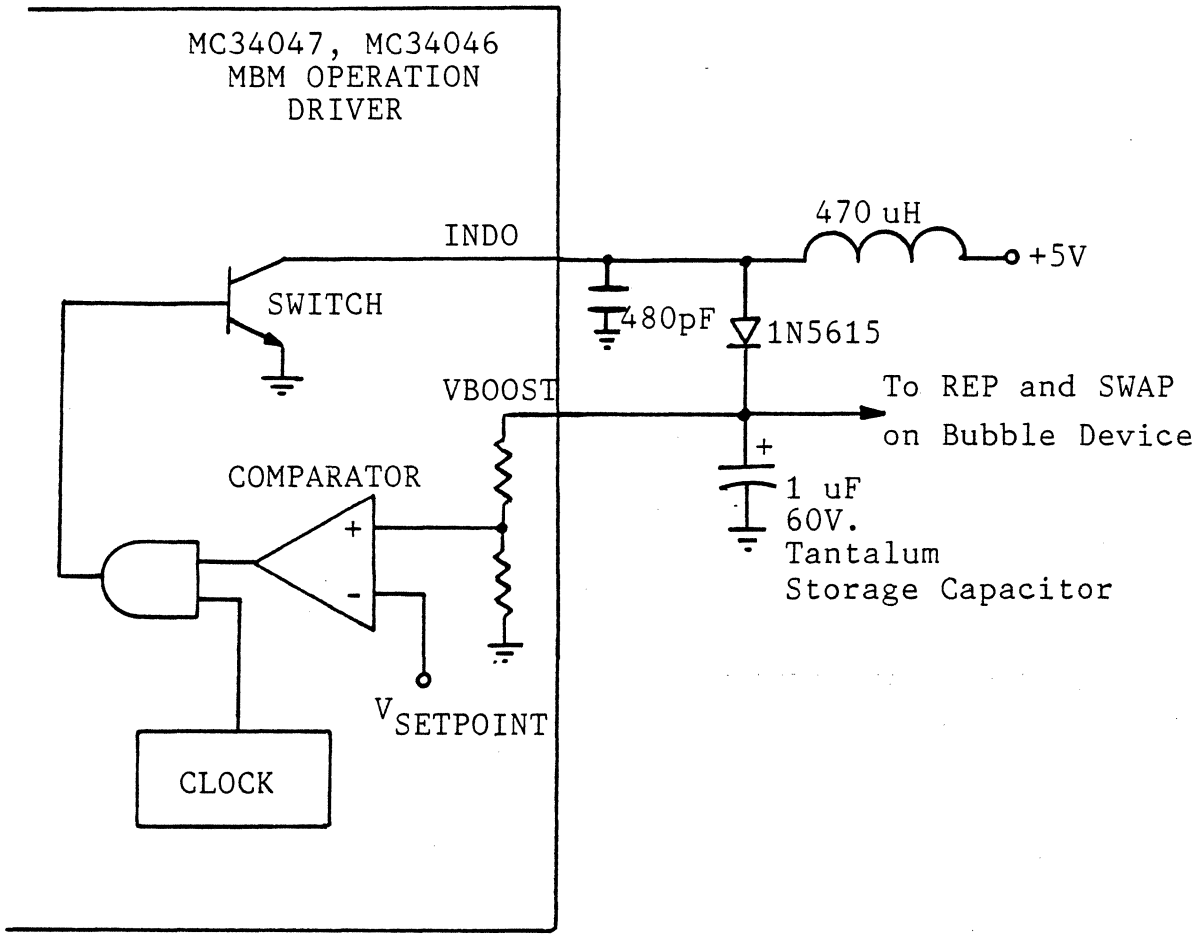


FIGURE 3.39

MBM OPERATION DRIVER VOLTAGE BOOSTER CIRCUIT

The operation of the voltage booster can be demonstrated with the model circuit of Figure 3.40. When the switch is closed, a ramped current is drawn through the inductor, L. As the switch is later opened, since the current in an inductor cannot change instantaneously, a high voltage is produced at the anode of the diode. This voltage forward-biases the diode and allows the storage capacitor, C, to be charged. When the produced voltage is low enough, the diode again becomes reverse-biased and the storage capacitor retains the high voltage. VBOOST on the MBM Operation Driver is used to sense the voltage across this capacitor and activate the switch for a predetermined amount of time whenever the booster voltage degrades below a certain value.

Figure 3.41 is a die photograph of the MBM Dual Operation Driver.

3.5 THE MBM SENSE AMPLIFIER

The MC34044 Bubble Memory Sense Amplifier is a bipolar monolithic integrated circuit designed to interface the differential detector output voltages of the MBM2256 and MBM2011 bubble memory devices with the TTL-compatible logic of the bubble memory subsystem. It is contained in a 14-pin dual-in-line package and is capable of directly interfacing to one pair of bubble memory detector outputs.

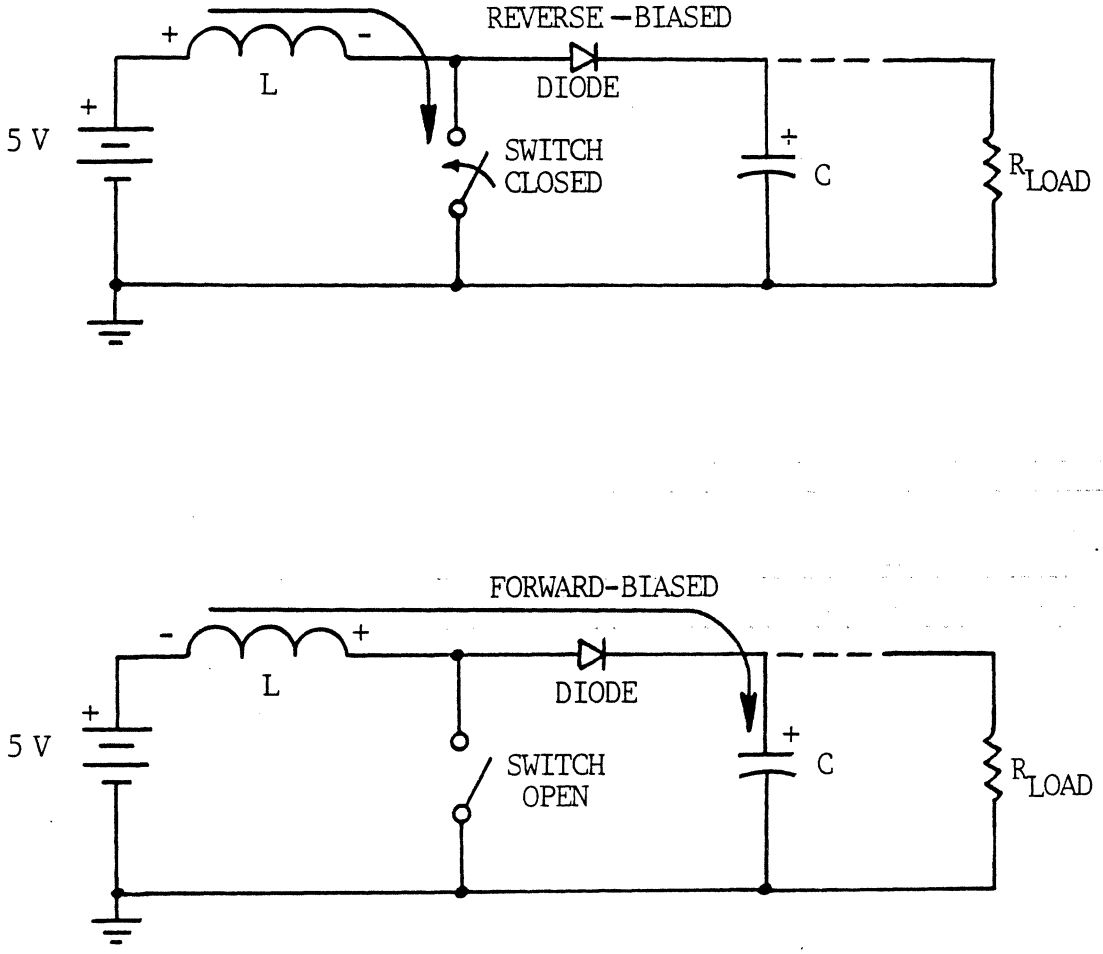


FIGURE 3.40

VOLTAGE BOOSTER MODEL CIRCUIT

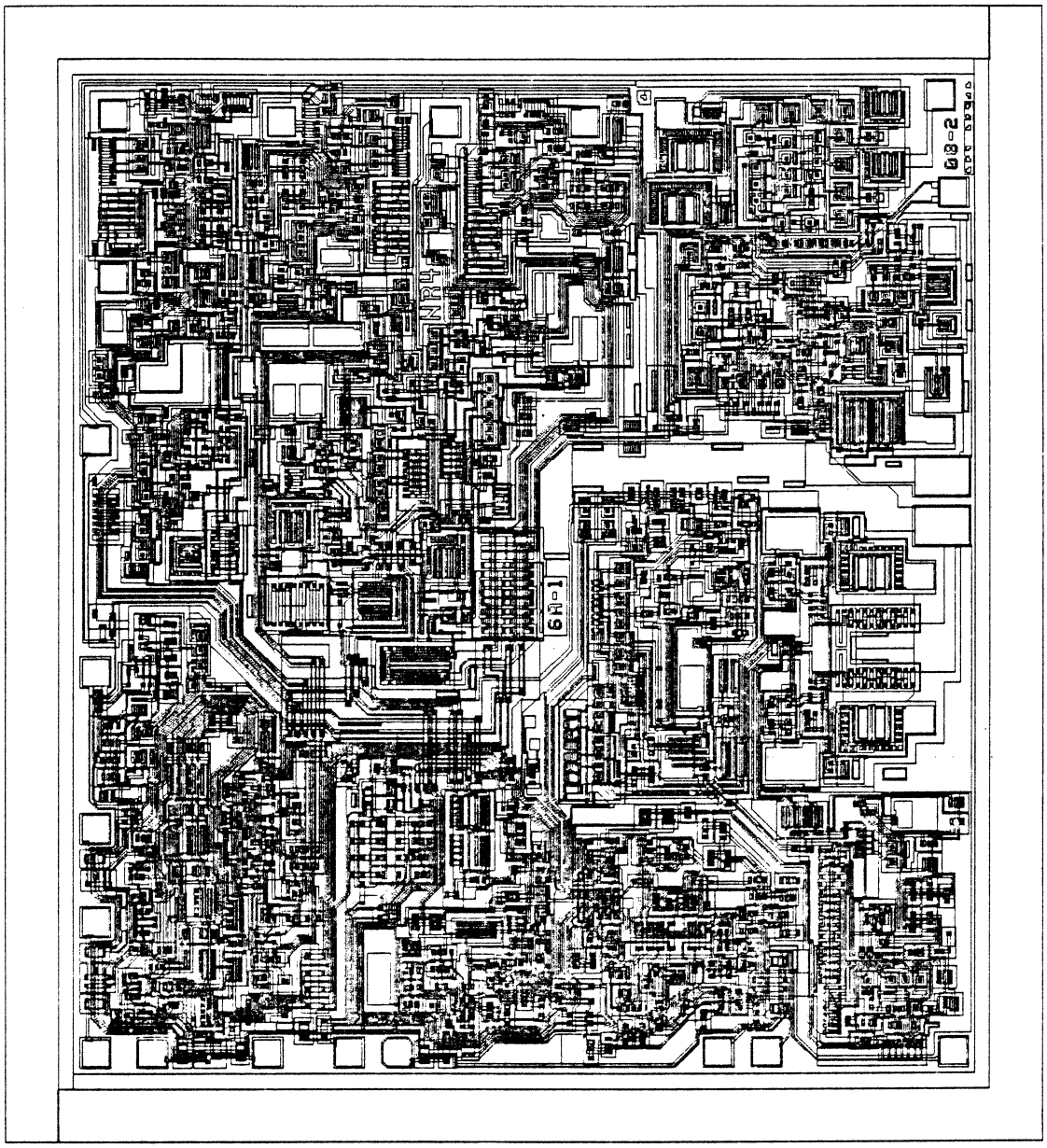


FIGURE 3.41

DUAL MBM OPERATION DRIVER DIE PHOTOGRAPH

The device features a true peak-to-peak sensing circuit, but also provides inputs for using an optional clamp and strobe sensing technique. Precision matched current sinks are included to provide the bubble memory device with the constant DC current required by the active and reference magnetoresistive detector elements. Both the bubble memory detector currents and sensing threshold voltages are externally adjustable. To provide for the capability of implementing a multiplexed, multiple-device bubble memory system, a separate chip select pin is available for this purpose. A single +12 volt supply and reference voltage are all that is required.

Reliable detection of bubble signals imposes serious constraints on the MBM sense amplifier, especially because bubble signals are inherently small in amplitude. Furthermore, differences between the resulting bubble signal and background uncancelled detector noise are on the order of several millivolts. System noise superimposed on supply voltages and/or grounds can typically reduce the signal-to-noise beyond that which is practically distinguishable if proper filtering is not provided. For this reason, the MBM sense amplifier has an on-chip high frequency ripple rejection regulator and noise compensation input that make it suitable for use in environments of high background noise and large AC common mode signals.

Figure 3.42 is a logic diagram of the MC34044 Bubble Memory Sense Amplifier. The IN+ and IN- pins should be connected to the active and reference detector elements, respectively. A resistor from the CSET pin to ground establishes a matched current flow through the detectors according to the equation:

$$I_D = \frac{10 \times V_{REF}}{R_{CSET}}$$

where, V_{REF} = 2.5 volts.

A threshold set pin, TSET, is provided to externally adjust the threshold voltage of the MBM Sense Amplifier. Figure 3.43 is a graph of the threshold voltage, V_{th}, as a function of the voltage applied to the TSET pin, V_{TSET}. Since the bubble detector output signal is heavily dependent upon the device temperature, temperature compensation of the threshold can be accomplished using a resistor and thermistor network.

The MBM controller provides a control signal, STROBE, which enables the sensing function of the MBM Sense Amplifier. This control signal is directly tied to both the CLAMP and STROBE inputs of the MBM Sense Amplifier. In this configuration, one channel of the MBM Sense Amplifier will search for and hold the most negative peak of the bubble memory detector signal within the STROBE window.

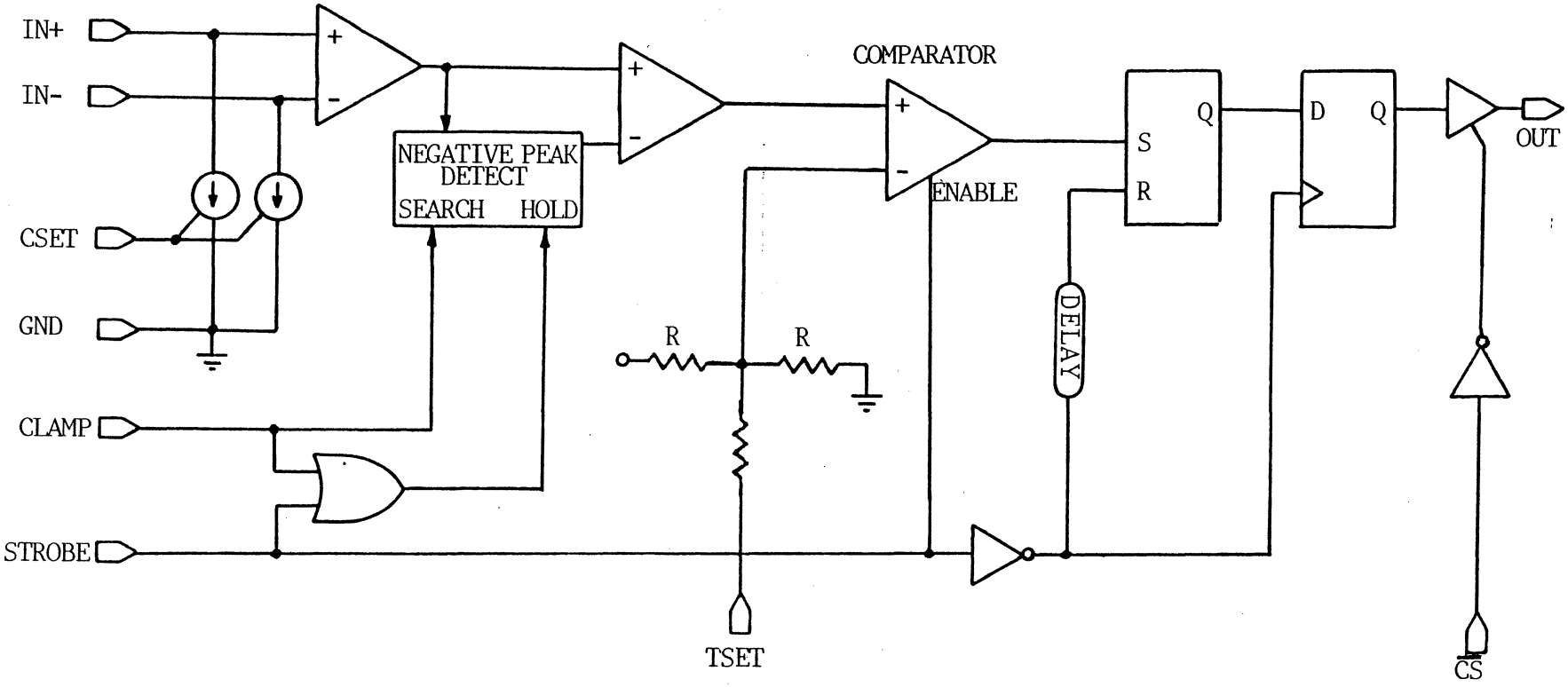


FIGURE 3.42

SENSE AMPLIFIER LOGIC DIAGRAM

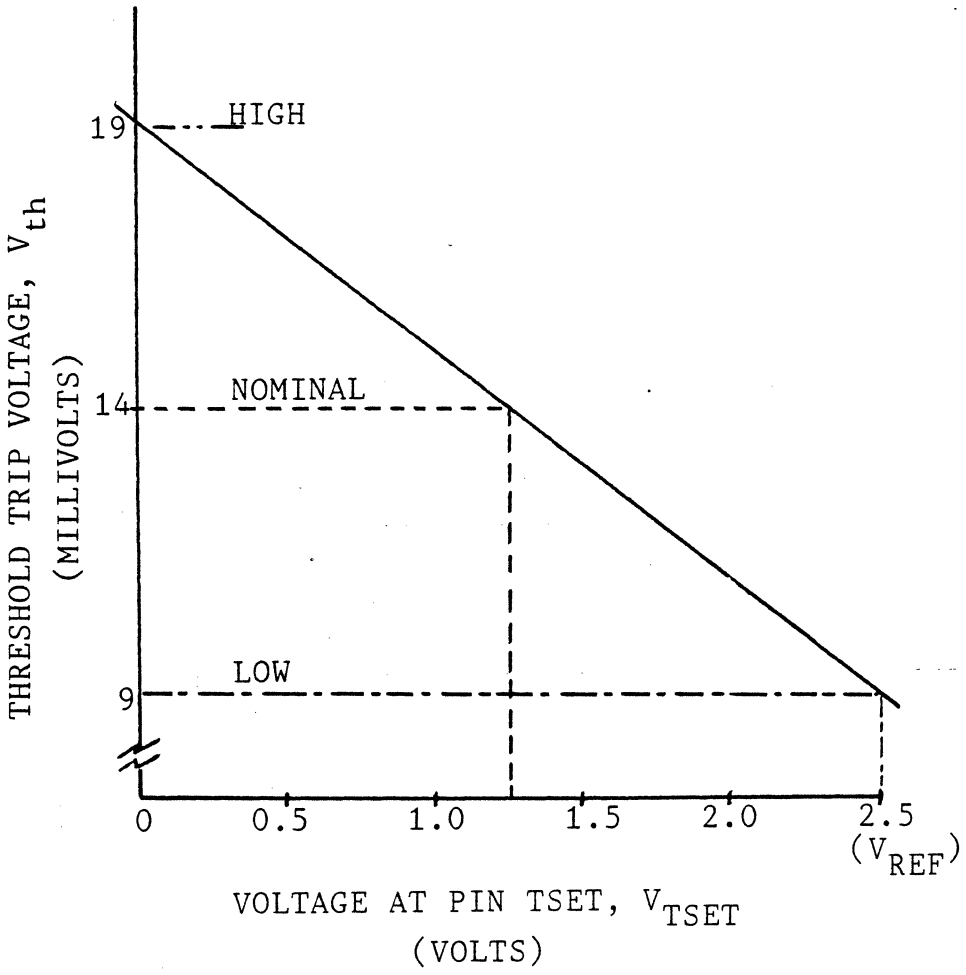


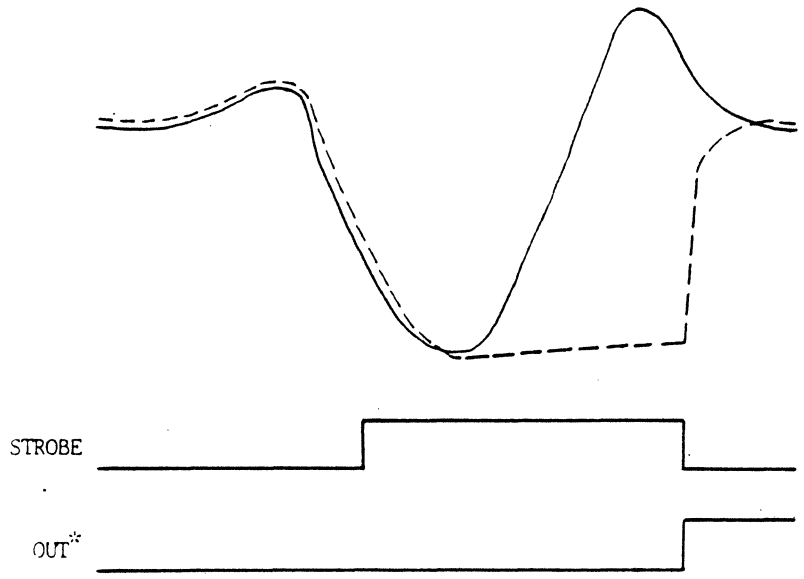
FIGURE 3.43

SENSE AMPLIFIER THRESHOLD ADJUSTMENT

The other channel follows the detector signal. See Figure 3.44. These two channels are compared during the STROBE window and providing the difference between the negative peak-hold channel and the signal-follow channel exceeds the threshold voltage, the MBM Sense Amplifier will output a TTL-compatible '1' signal at the trailing edge of STROBE.

Figure 3.45 shows the use of the MBM Sense Amplifier with a CLAMP (actually an unclamp operation) and STROBE sensing scheme. (Note that the MBM controller does not support this mode of operation.) This mode of operation is particularily well-suited for very noisy environments. Any induced noise spikes can be effectively blocked out by placing the CLAMP and STROBE timings appropriately. Then, the negative search and hold function will be enabled throughout CLAMP, while the negative peak hold operation will be sustained until the trailing edge of STROBE. The compare operation of the hold signal channel, the follow signal channel, and the threshold is then enabled by the STROBE signal.

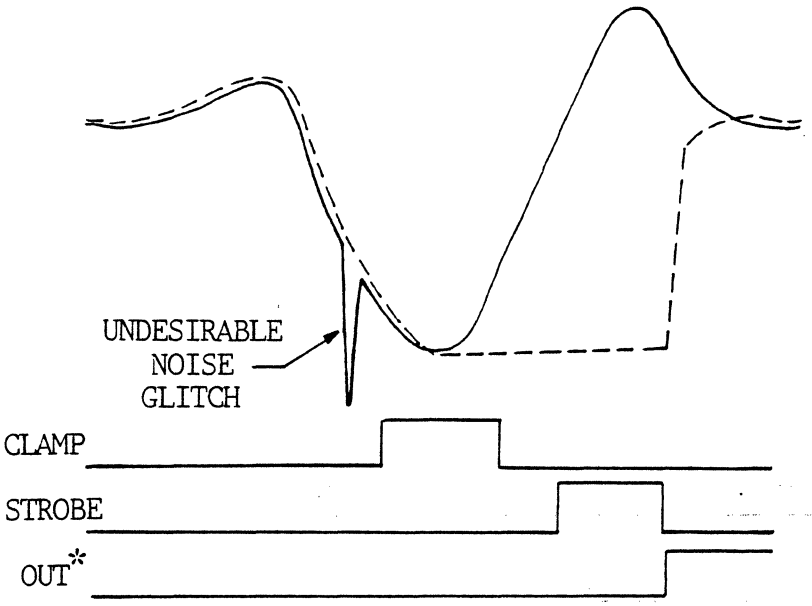
The MBM Sense Amplifier die photograph is given in Figure 3.46.



*Assuming previous data bit was a logic '0'.

FIGURE 3.44

PEAK-TO-PEAK SENSING SCHEME



*Assuming previous data bit was a logic '0'.

FIGURE 3.45

CLAMP AND STROBE SENSING SCHEME

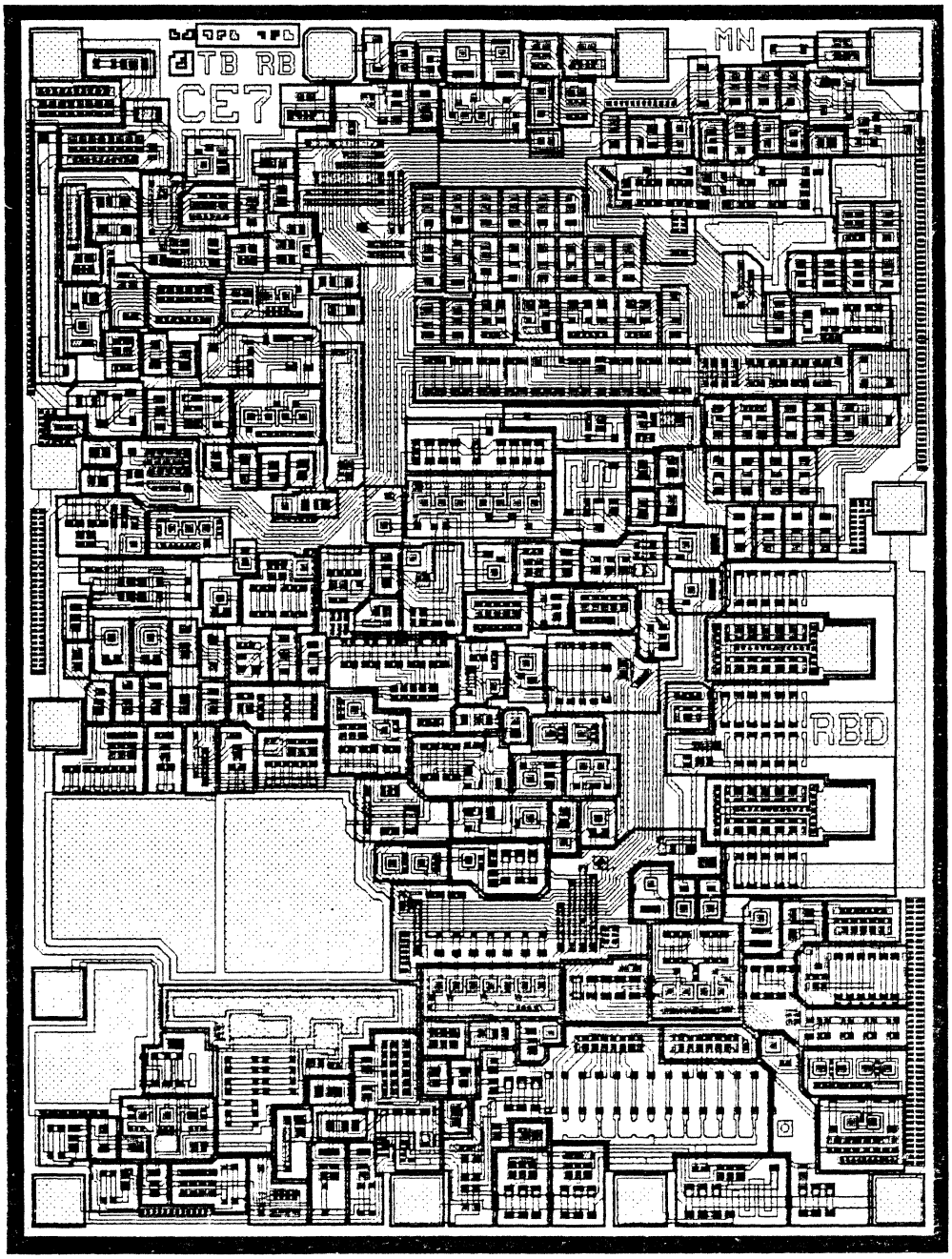


FIGURE 3.46

MBM SENSE AMPLIFIER DIE PHOTOGRAPH

CHAPTER 4

MBM SYSTEM CONFIGURATIONS

There are a number of allowable system configurations using the bubble memories, support circuits, and controllers discussed in Chapter 3. They range in complexity from the minimum system consisting of a single bubble memory device with a single set of support circuits and one MBM controller to systems using multiple MBM subsystems and multiple MBM controllers. The purpose of this chapter, therefore, is to present the available options to the system designer along with the inherent advantages and disadvantages of each configuration.

4.1 THE MINIMUM MBM SYSTEM

Figure 4.1 is a block diagram of the minimum MBM system configuration. As shown, the system consists of one bubble memory device, one each of the MBM support circuits (this comprises the MBM subsystem) and an MBM controller.

In this configuration, the MBM controller outputs serial write data on its DOUT pin at a rate equal to that of the MBM propagation cycle (i.e., 100 Kbit/s for the 1 Mbit MBM and 125 Kbit/s for the 256 Kbit MBM). The

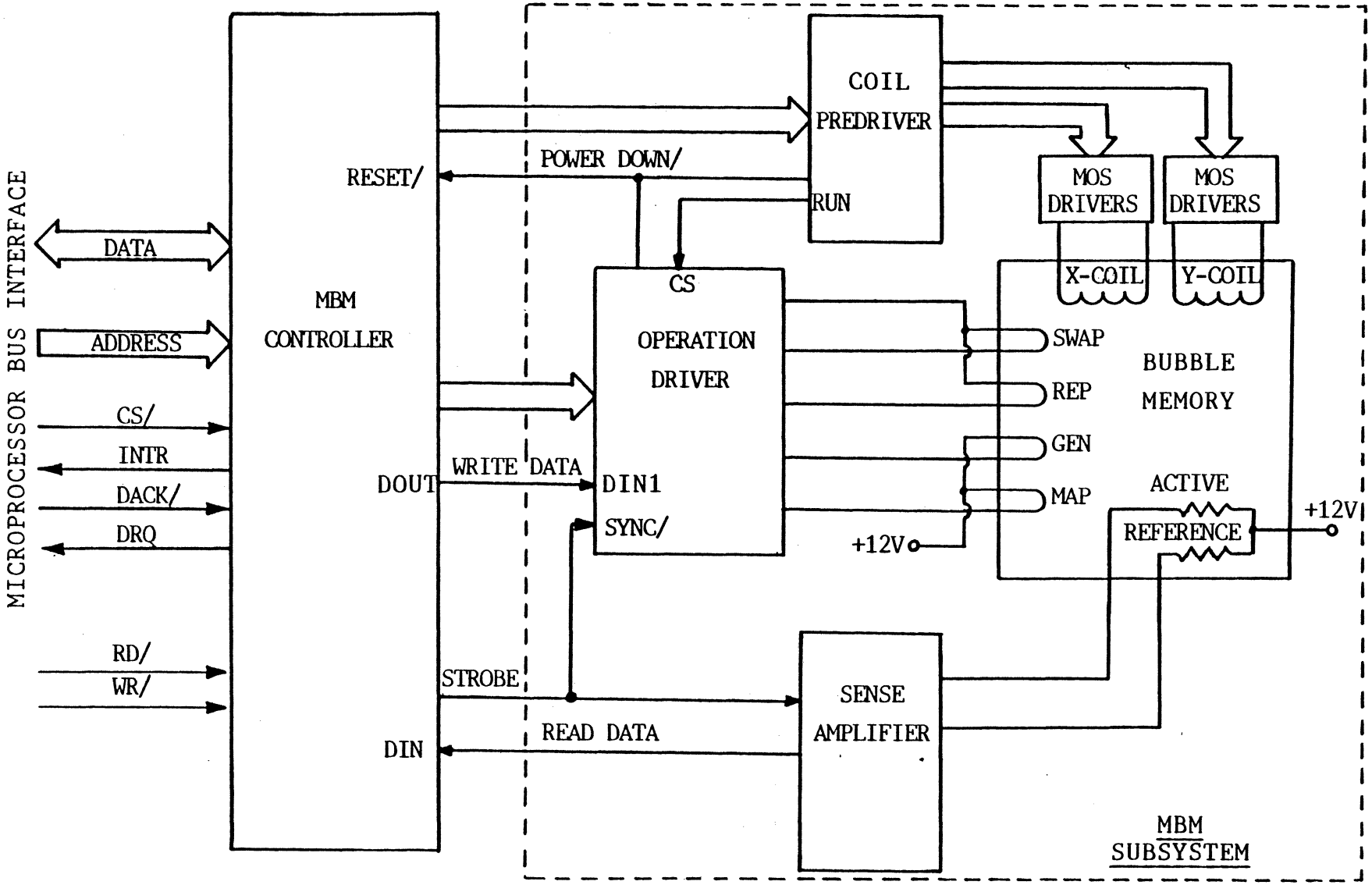


FIGURE 4.1

MINIMUM SYSTEM BLOCK DIAGRAM

MBM controller signal, STROBE, latches the write data into the MBM Operation Driver at its rising edge. The MBM Operation Driver, in turn, outputs the controlled generate current on the following MBM propagation cycle when the GEN signal is received, provided that the data bit latched was a logic high level. (Hence, the MBM controller GEN signal controls the phase of the generate current pulse, while the MBM Operation Driver controls the signal amplitude, rise time and slow decay time.)

During the MBM read operations, the STROBE signal trailing edge clocks the serial digital read data out of the MBM Sense Amplifier OUT pin into the MBM Controller DIN pin, again at the same rate as the MBM propagation cycle.

Therefore, the burst subsystem data rate for the 1 Mbit (256 Kbit) minimum system is 100 Kbit/s (125 Kbit/s). This translates to a burst transfer rate over the user's system interface of 12.5 KByte/s (15.6 KByte/s). Taking redundant loops, interpage gaps and the ECC overhead into account, the average data transfer rate can then be calculated as follows:

$$\text{Ave. User Transfer Rate } (UTR_{ave}) = \frac{\text{Number of Data Bits}}{\text{Interpage Spacing}} \times \text{Burst Rate}$$

$$UTR_{ave}(1M) = \frac{512}{601} \times 12.5 \text{ KByte/s}$$

$$= 10.6 \text{ KByte/s}$$

and,

$$UTR_{ave}(256K) = \frac{512}{594} \times 15.6 \text{ KByte/s}$$

$$= 13.4 \text{ KByte/s}$$

The one-device MBM system, therefore, has a relatively low to moderate average transfer rate. It has the advantage of being light-weight, physically small (a one megabit MBM system in minimum configuration occupies less than 12 square inches of board area), and relatively low in power consumption.

Motorola's MBM2011EK one megabit Bubble Memory Evaluation Kit is shown in Figure 4.2. The board dimensions, including the edge connector, are only 3.4 x 3.5 x 0.5 inches. Maximum standby power dissipation is specified at 2 watts, while the maximum active power dissipation (measured at 100% duty cycle) is less than 4 watts. Certainly, since the bubble memory is a non-volatile storage medium, the power can be disconnected when periods between bubble memory accesses are excessively long.

Figure 4.3 is a schematic diagram for the MBM2011EK and Figure 4.4 shows the board layout for this bubble memory system.

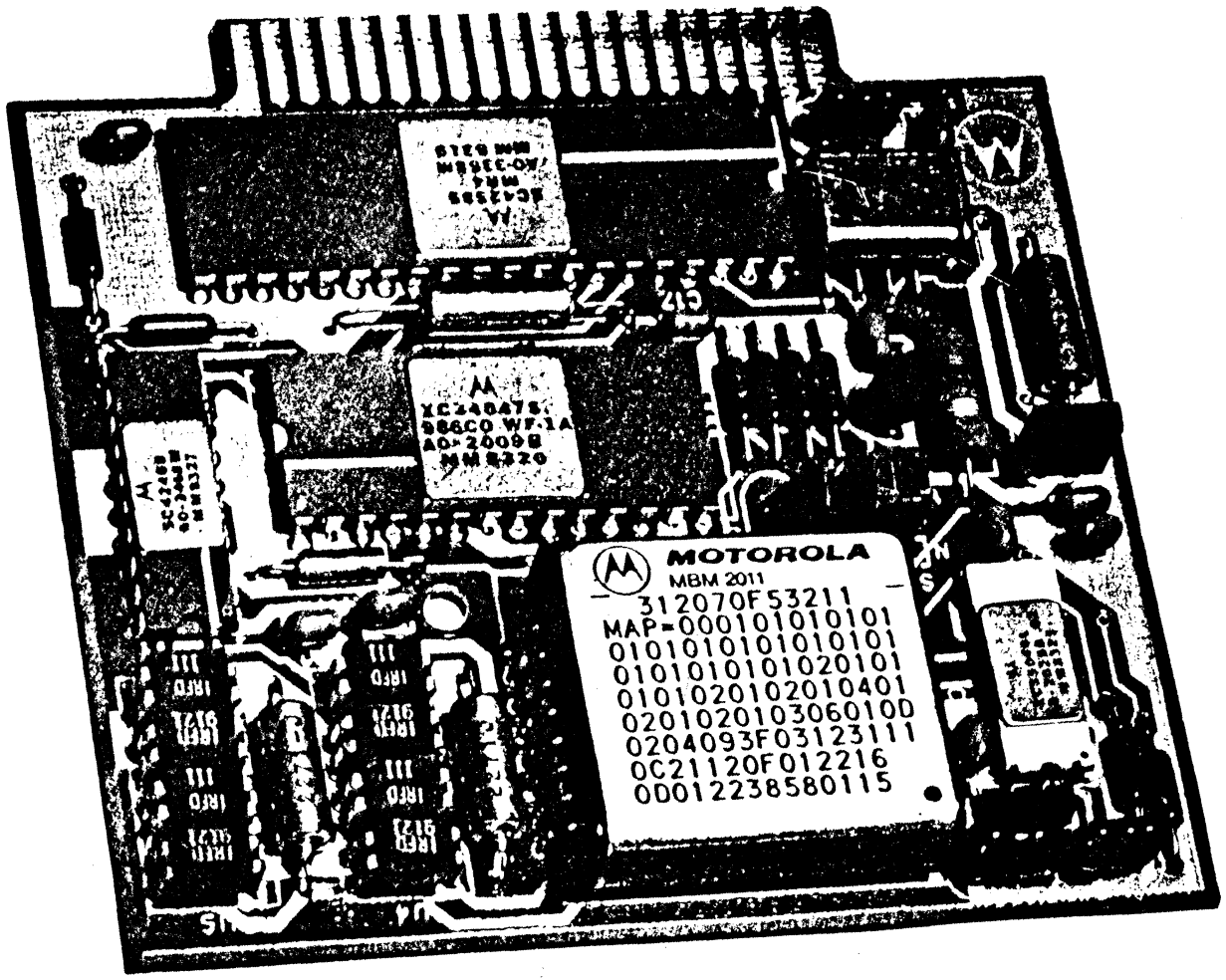
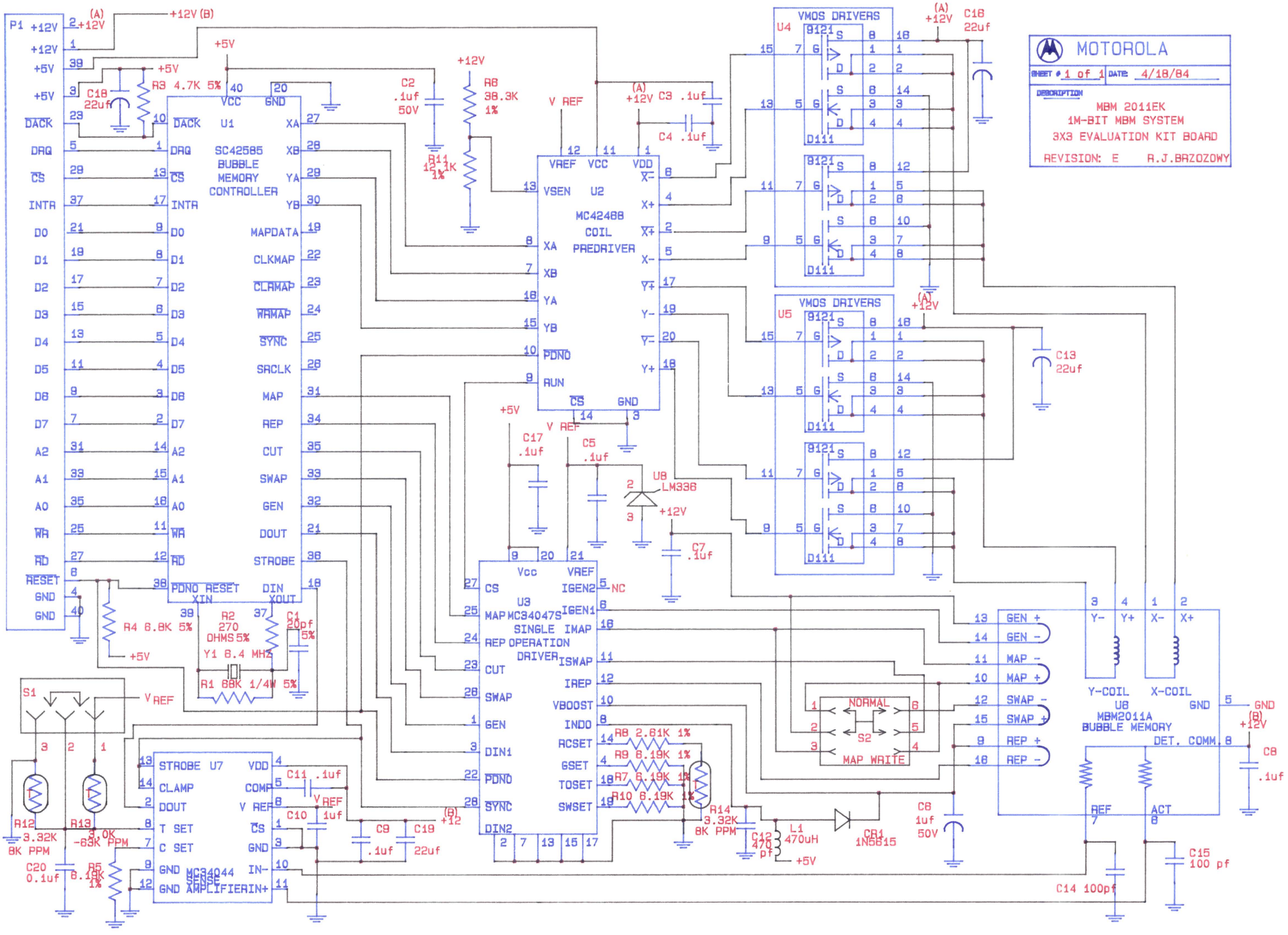


FIGURE 4.2

MOTOROLA'S MBM2011EK 1MBIT EVALUATION KIT

FIGURE 4.3

MBM2011EK SYSTEM SCHEMATIC


MOTOROLA
SHEET # 1 of 1
DATE 4/18/84
DESCRIPTION
MBM 2011EK
1M-BIT MBM SYSTEM
3X3 EVALUATION KIT BOARD
REVISION: E R.J.BRZOZOWY
P1
U1
SC42585
BUBBLE
MEMORY
CONTROLLER
U2
MC42488
COIL
PREDRIVER
U3
MC34047S
SINGLE IMAP
OPERATION
DRIVER
U4
VMOS DRIVERS
U5
VMOS DRIVERS
U6
MBM2011A
BUBBLE MEMORY
U7
MC34044
SENSE
AMPLIFIER
U8
LM336
Y-COIL
X-COIL
NORMAL
MAP WRITE
S1
S2
Y1 8.4 MHZ
R1 68K 1/4W 5%
R2 270 OHMS 5%
R3 4.7K 5%
R4 6.8K 5%
R5 6.19K 1%
R6 38.3K 1%
R7 6.19K 1%
R8 2.61K 1%
R9 6.19K 1%
R10 6.19K 1%
R11 12.1K 1%
R12 3.32K 8K PPM
R13 3.0K -63K PPM
R14 3.32K 8K PPM
C1 20pf 5%
C2 .1uf 50V
C3 .1uf
C4 .1uf
C5 .1uf
C7 .1uf
C8 1uf 50V
C9 .1uf
C10 1uf
C11 .1uf
C12 470 pf
C13 22uf
C14 100pf
C15 100 pf
C16 22uf
C17 .1uf
C18 22uf
C19 22uf
C20 0.1uf
L1 470uH
CR1 1N5815
+12V (A)
+12V (B)
+5V
V REF
GND

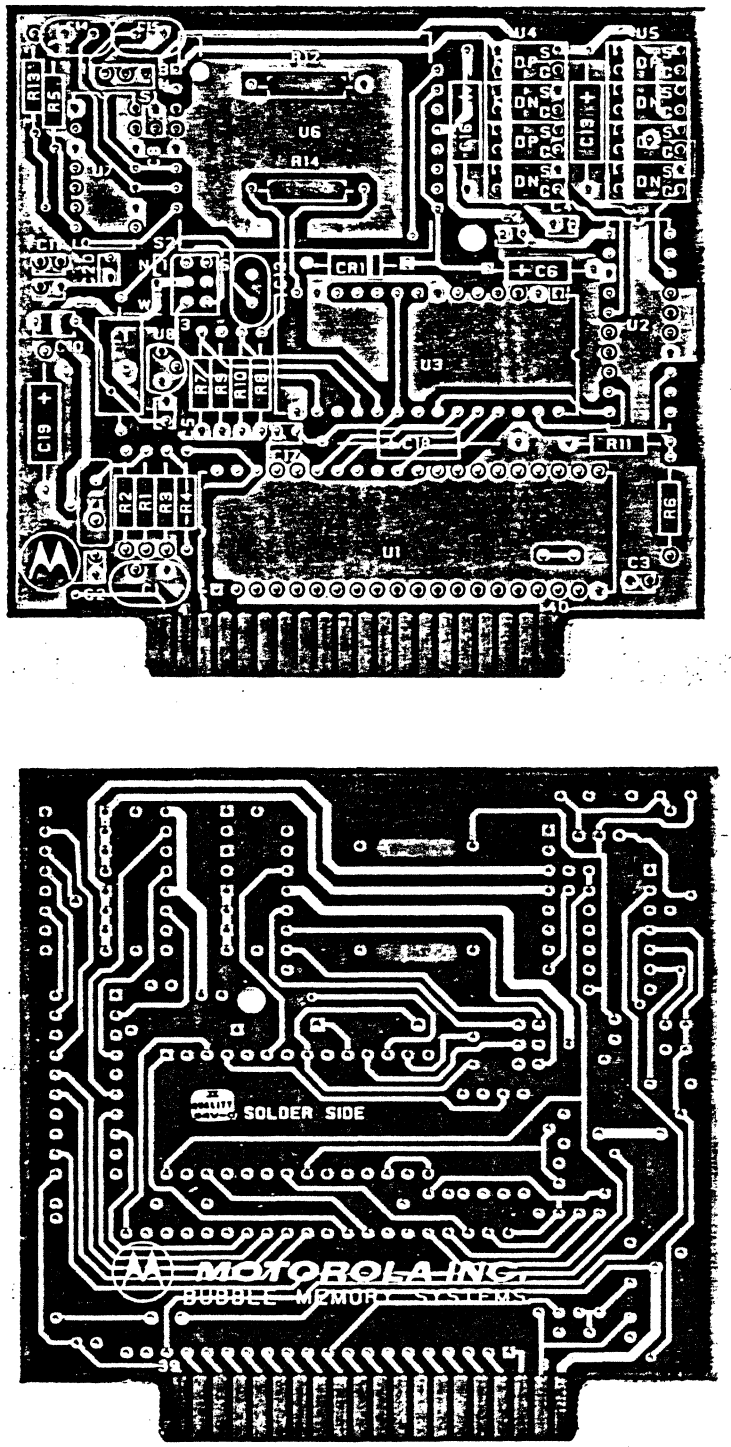


FIGURE 4.4

EVALUATION KIT BOARD LAYOUT

4.2 PARALLEL MBM SYSTEMS

As mentioned in Chapter 3, the MBM controller is designed to operate 2, 4, or 8 bubble memories in parallel, in addition to the single MBM operation discussed in Section 4.1. This parallel operation is accomplished using some additional circuitry in the configuration illustrated in Figure 4.5.

The MBM controller is informed of the number of parallel MBM subsystems it is operating when the user loads the System Features Register bits SFRØ and SFR1. There is basically no difference between the MBM subsystem of the minimum system configuration and the MBM subsystems shown in Figure 4.5, except that a Dual MBM Operation Driver can be shared by two MBM subsystems in the parallel mode.

Each subsystem operates synchronously with each other. The difference lies in the increased burst data rate of the MBM controller DOUT and DIN lines. In the minimum configuration, the MBM controller outputs and inputs data at a rate of one bit per MBM propagation cycle. In the parallel MBM system, however, data is output and sampled at its input at eight times the MBM propagation cycle. A shift clock, SRCLK, is provided for shifting data to and from the serial-to-parallel and parallel-to-serial

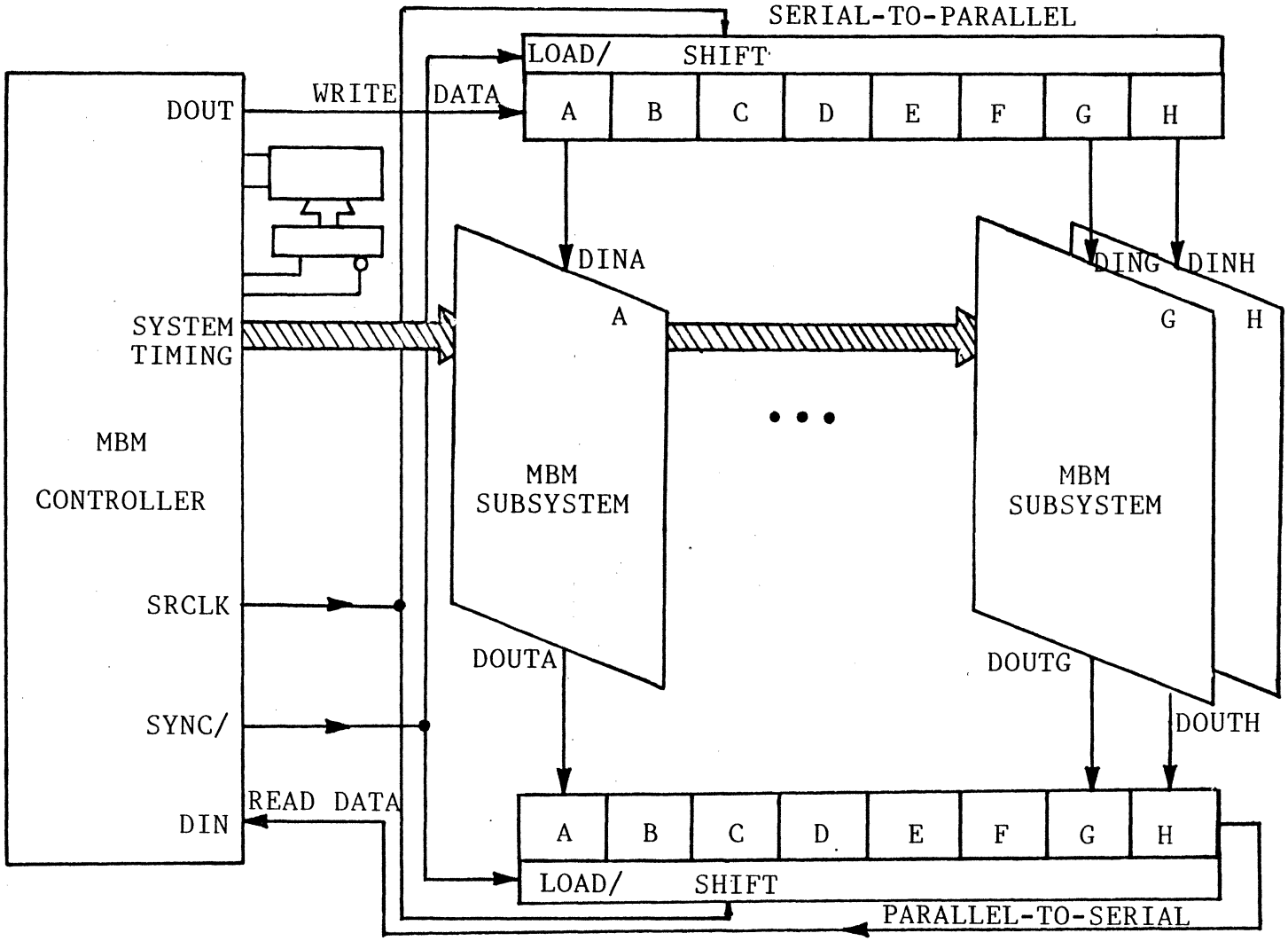


FIGURE 4.5

PARALLEL OPERATION OF MBM SUBSYSTEMS

shift registers shown in Figure 4.5. Naturally, SRCLK operates at a frequency at eight times the MBM propagation frequency (i.e., 800 KHz for the 1 Mbit and 1 MHz for the 256 Kbit systems).

During the MBM write operation, the controller outputs serial data on DOUT. This data is shifted into a serial-to-parallel converter (e.g., 74LS164) by SRCLK. Every eighth SRCLK pulse, SYNC/ (connected to the MBM operation drivers and shift registers) loads the data from the serial-to-parallel converter into the eight MBM subsystems simultaneously. This data is then written into the eight MBM's in parallel while the subsequent eight bits of data are being shifted into the serial-to-parallel converter.

Likewise, during the MBM read operations, data are presented to the parallel-to-serial converter (e.g., 74LS165) by each of the MBM sense amplifiers of each of the MBM subsystems. SYNC/ loads the parallel data and SRCLK shifts it serially into DIN on the controller, again at eight times the MBM propagation rate.

A four-device MBM parallel system is thus formed by using the MBM subsystem positions denoted E through H of Figure 4.5. A two-device MBM parallel system is formed by using the MBM subsystem positions denoted G and H. The burst data rate for two- and four-MBM parallel systems

remains at eight times the MBM propagation rate, however, data is clocked out and in of the MBM controller for only the first two and first four SRCLKs, respectively.

Figure 4.6 is a timing diagram showing the use of the DOUT and DIN controller lines in the parallel subsystem mode for 1, 2, 4 and 8 bubble memory subsystems operating in parallel.

In the minimum system configuration, the RMPI for the bubble memory is stored in the internal MAP RAM (594 bits) of the MBM controller (as is the RMPI of a two-device 256K MBM system). However, in multiple-device MBM systems, where the RMPI of all the MBMs (2, 4, or 8) must be stored, there is not sufficient storage space available in the internal MAP RAM. Therefore, the controller provides timing signals to store additional RMPI (once the internal MAP RAM overflows) in an external RAM (or PROM, if desired). The circuitry required to support this external MAP RAM storage is illustrated in Figure 4.7.

When the external MAP RAM is to be addressed, the CLRMAP/ signal clears the counters, which act as current address pointers to the RAM memory locations. CLKMAP increments the counter and WRMAP/ writes data to the external map from the DIN line during the MBM system initialization process.

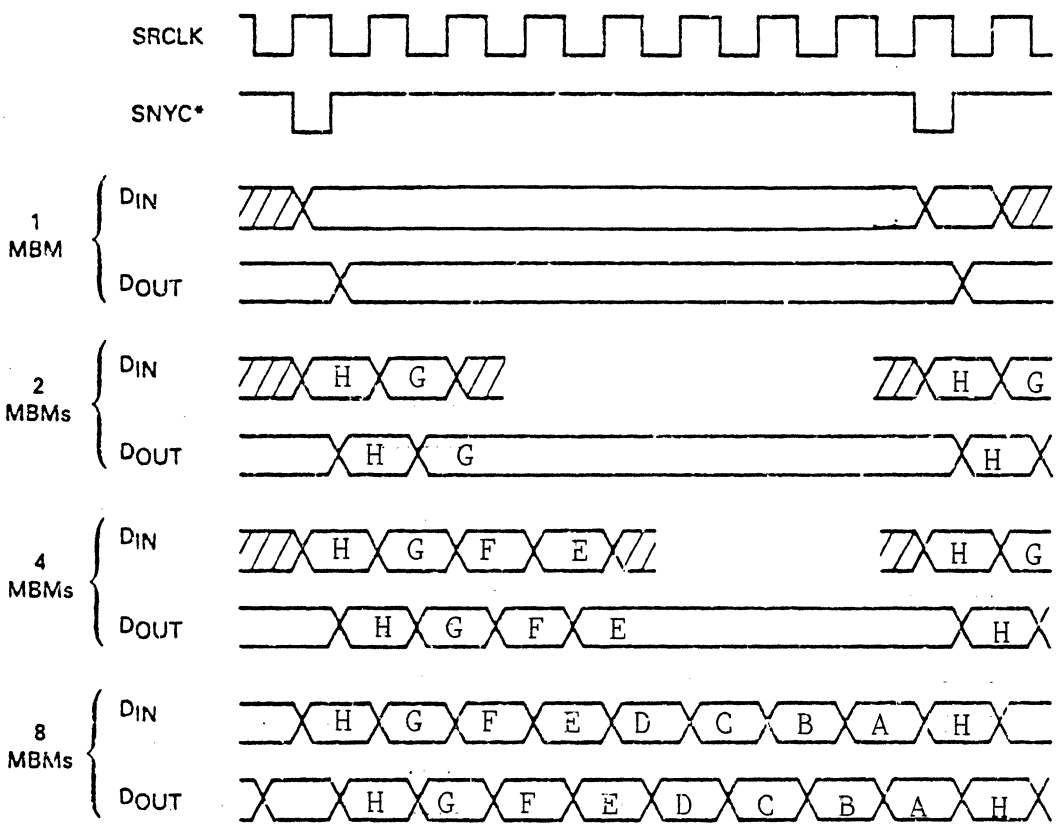


FIGURE 4.6

READ AND WRITE DATA TIMING

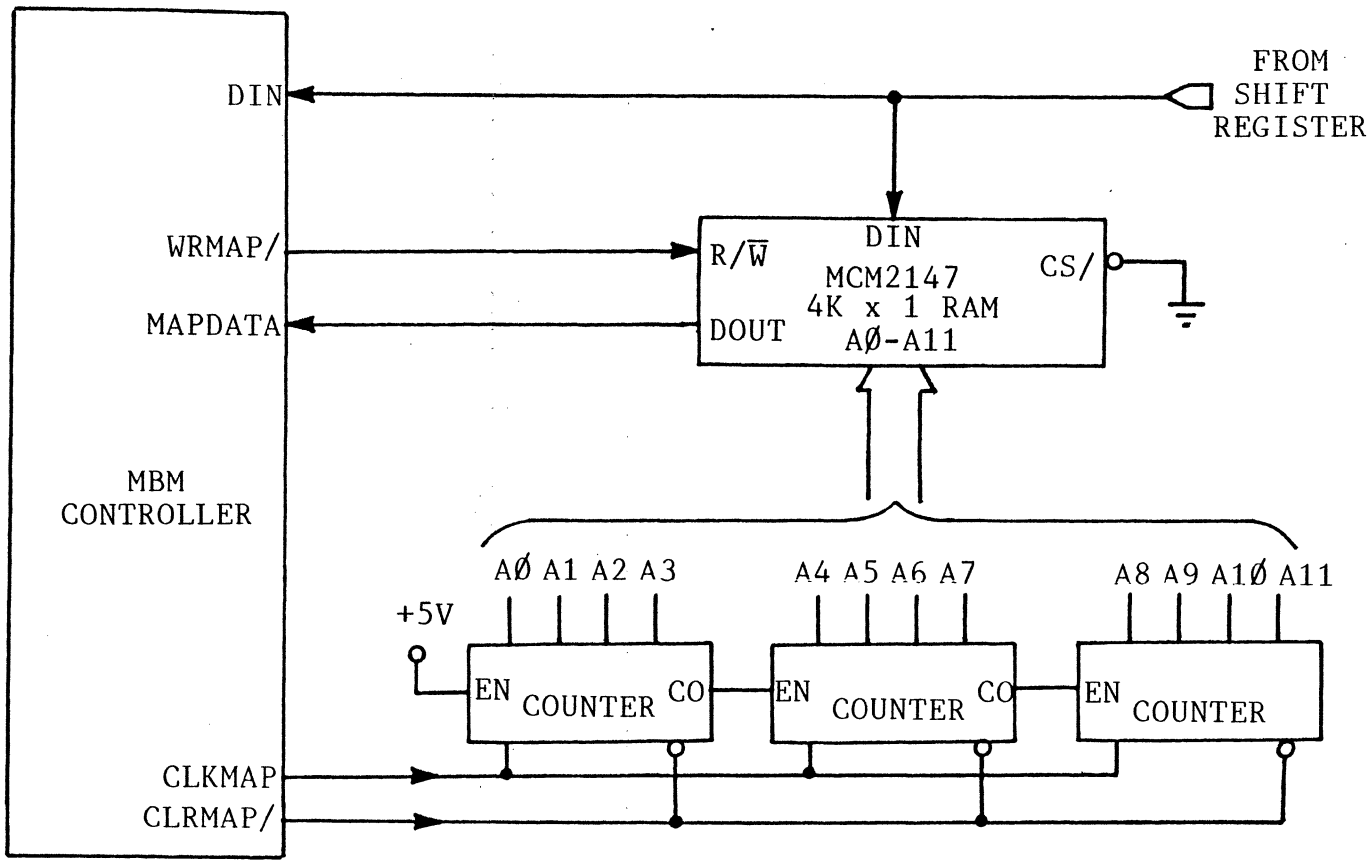


FIGURE 4.7

EXTERNAL MAP RAM CIRCUITRY

When data is being read from or written to the MBM subsystems, the counters are cleared by CLRMAP/ and the controller clocks the counters and samples MAPDATA, when necessary, to determine the redundant loop positions in each of the MBM subsystems. During the initialization process, the RMPI of the parallel MBM subsystems is interleaved following the loading of the parallel-to-serial shift register. Thus, redundant loop positions for an individual MBM subsystem correspond to a certain bit position in the 524 x N record (i.e., page) of data, where N = the number of MBMs in parallel. The required MAP RAM storage capacity for 1, 2, 4, and 8 parallel MBM systems (both 256 Kbit and 1 Mbit) is given in Table 4.1. Figure 4.8 is a timing diagram which shows the operation of the MBM controller external MAP RAM control signals for 1, 2, 4, and 8 MBMs operating in parallel.

Figure 4.9 is a photograph of a four-device parallel megabit bubble memory system prototype. Total memory storage capacity is, therefore, 512 KBytes. It uses four MBM2011 bubble memory devices, four SC42468 coil predrivers, eight coil drivers, four MC34044 sense amplifiers, two dual MBM operation drivers, and one MBM controller. External MAP RAM circuitry, interface circuitry, relocatable address switches, and program PROMs are also provided on the board, which plugs directly into Motorola's EXORbus.® Figure 4.10 is a schematic for a two-device MBM system.

256K (1M)

# MBMs	USING INTERNAL MAP RAM	NOT USING INTERNAL MAP RAM
1	0 (0)	282 (584)
2	0 (574)	564 (1168)
4	534 (1742)	1128 (2336)
8	1662 (4078)	2256 (4672)

256K => #RMPI bits = N x 282 - I(594)

1M => #RMPI bits = N x 584 - I(594)

where N = the number of parallel MBM subsystems

I = 0, when not using internal MAP RAM

I = 1, when using internal MAP RAM

TABLE 4.1

REQUIRED EXTERNAL MAP RAM CAPACITIES

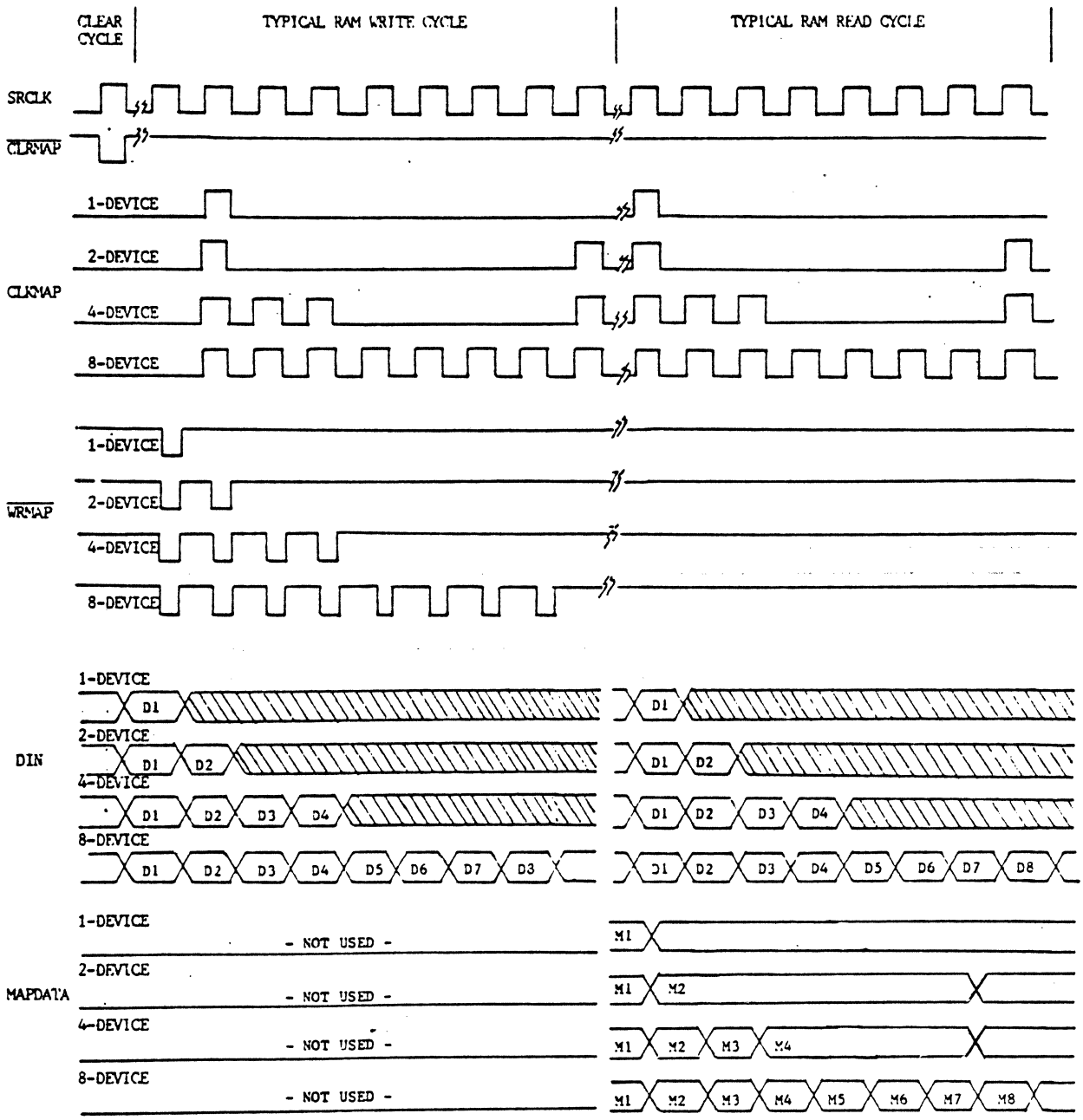


FIGURE 4.8

EXTERNAL MAP RAM TIMING

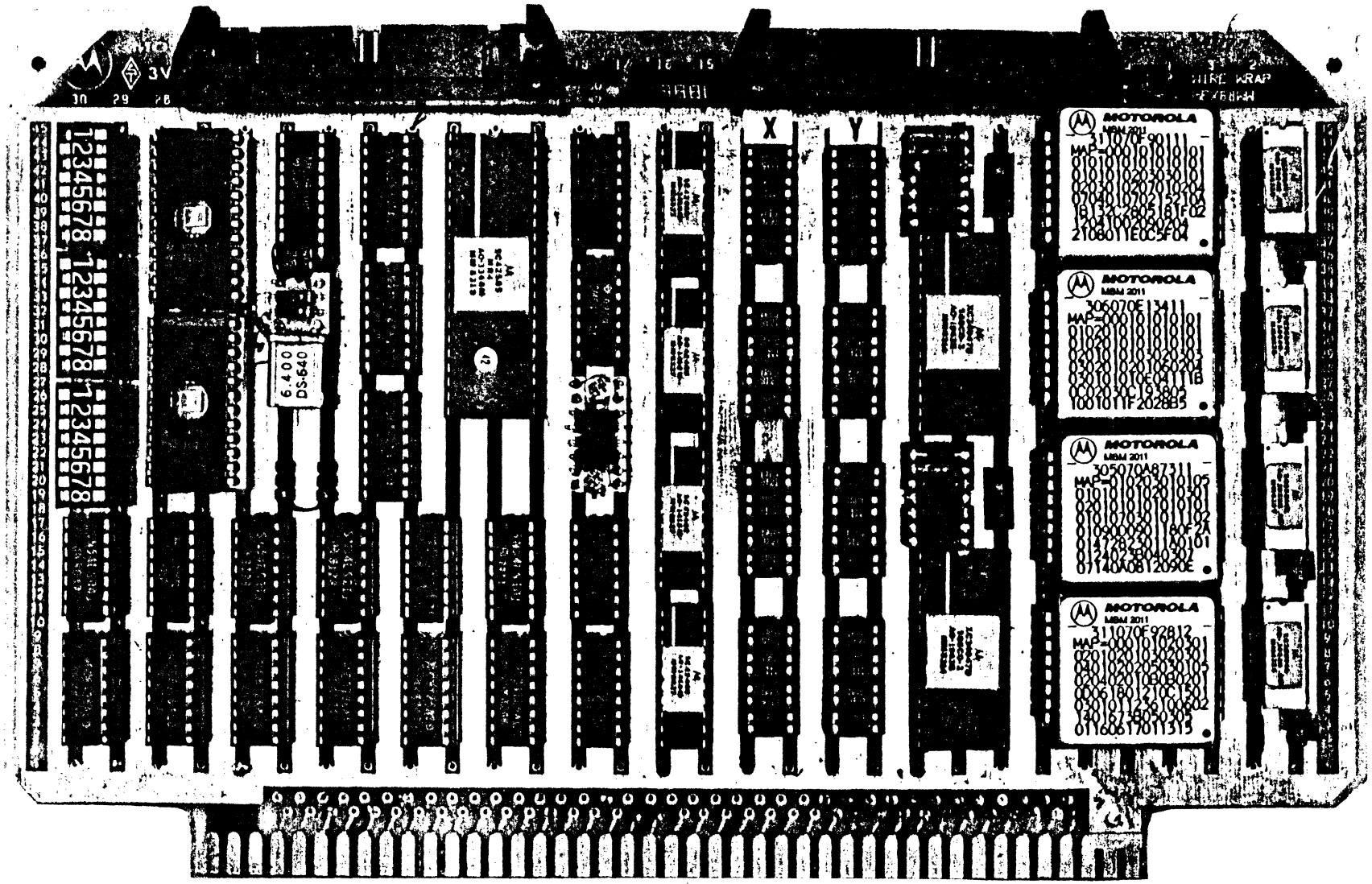


FIGURE 4.9

4-DEVICE PARALLEL MBM SYSTEM (512KB)

FIGURE 4.10

2-DEVICE PARALLEL MBM SYSTEM SCHEMATIC

MOTOROLA
BUBBLE MEMORY SYSTEMS
SHEET 1 of 1 DATE APRIL 28, 1984
DESCRIPTION
2-DEVICE MBM SYSTEM
REVISION: A R.J. BRZOZOWY

4K X 1 RAM
R/W
DOUT
DIN
A0-A11
A0-A11 COUNTER
CLK
CLR

+5V
+12V
22uf 20V
88.8K 1%
12.1K 1%
8.8K 5%
VREF +5V +12V
VREF VCC VDD
VSEN U2
MC42488 COIL PREDRIVER
XA XB YA YB PDNO RUN
X- X+ X+ X- Y+ Y- Y- Y+
CS GND

VMOS DRIVERS
D111

+5V
40 20
VCC GND
DACR U1 SC42866 BUBBLE MEMORY CONTROLLER
DRQ CS INTR D0 D1 D2 D3 D4 D5 D6 D7 A2 A1 A0 WR RD PDNO RESET
XA XB YA YB MAPDATA CLKMAP CCRMAP WRMAP SYNC SRCLK MAP REP CUT SWAP GEN DOUT STROBE DIN
XIN XOUT
88K 270 8.4MHz 20pf

74LS164
IN A B C D E F G H
CLK LOAD/
SERIAL-TO-PARALLEL SR

74LS165
A B C D E F G H OUT
CLK LOAD/
PARALLEL-TO-SERIAL SR

AND

+5V VREF
Vcc VREF
U8 MC34047D DUAL OPERATION DRIVER
CS MAP REP CUT SWAP GEN DIN1 PDNO SYNC DIN2
IGEN2 IGEN1 IMAP ISWAP IREP VBOOST INDO RCSET RSET TCSET SWSET
1uf 80V
1N5815
470uH
8.19K 1%
2.81K 1%
8.82K
8.3K ppm

GEN + GEN - MAP - MAP + SWAP - SWAP + REP + REP -
Y- Y+ X- X+
Y-COIL X-COIL GND
U8 MBM2011A BUBBLE MEMORY
DET. COMM.
REF ACT
3K -88K ppm
8.82K
8.8K ppm
8.19K 1%
.1uf

STROBE U7 CLAMP DOUT T SET C SET GND
MC34044 SENSE AMPLIFIER
VDD COMP V REF CS GND IN- IN+
.1uf
1uf
100pf

As discussed in Chapter 3, the sector size is set and does not vary with the number of MBMs operating in parallel. The page size, however, changes with the number of MBMs operating in parallel as shown in Table 4.2.

Parallel MBM systems have the advantage of high data transfer rates, but at the same time, they require more power to operate and naturally have a higher system component count. Access times are equal to that of the minimum system configuration. Table 4.3 shows the required component count for 1, 2, 4 and 8 MBMs in the parallel mode. Also listed is the resultant memory capacity per package.

Table 4.4 lists the typical power requirements of the bubble memory system when operating 1, 2, 4 or 8 bubble memory subsystems.

4.3 MULTIPLEXED MBM SYSTEMS

Figure 4.11 shows the configuration of a typical multiplexed multiple-MBM system. Select circuitry is provided to enable only a single MBM subsystem at any one time. When the MBM subsystems are deselected, the MBM sense amplifier output is tri-stated and the MBM operation driver (each subsystem has its own) and coil predriver will not respond to control signals at their inputs. Therefore, the read and write data lines of each of the MBM subsystems

	256K				1M			
# MBMs	SECTOR SIZE (bits)	# SECTORS	PAGE SIZE (bits)	# PAGES	SECTOR SIZE (bits)	# SECTORS	PAGE SIZE (bits)	# PAGES
1	2048	128	512*	512*	4096	256	512	2048
2	2048	256	512	1024	4096	512	1024	2048
4	2048	512	1024	1024	4096	1024	2048	2048
8	2048	1024	2048	1024	4096	2048	4096	2048

*A one-device 256K MBM system must perform two swaps and two replicates to fulfill the requirements of the 524-bit ECC block.

TABLE 4.2

SECTOR AND PAGE ADDRESSING

PARALLEL-MODE

MBM SYSTEM COMPONENT COUNT

256K (1M)

TOTAL MEMORY CAPACITY (BYTES)	MBMs REQUIRED	SUPPORT CIRCUITS REQUIRED	CONTROL-LERS REQUIRED	SHIFT REGS AND EXTERNAL MAP RAM	TOTAL	AVE. Kbits PER PACKAGE
32K (128K)	1	5	1	0	7	36.6 (143)
64K (256K)	2	9	1	2 (6)	14 (18)	36.6 (111)
128K (512K)	4	18	1	6	29	35.3 (138)
256K (1M)	8	36	1	6	51	40.2 (157)

TABLE 4.3

PARALLEL SYSTEM COMPONENT COUNT

POWER (WATTS)
(1 Mbit)

# MBMs	STANDBY	ACTIVE (100% duty cycle)
1	1.67	3.60
2	2.35	6.20
4	4.12	11.81
8	7.65	23.02

NOTE: Measurements made at 25°C.

TABLE 4.4

TYPICAL POWER DISSIPATION

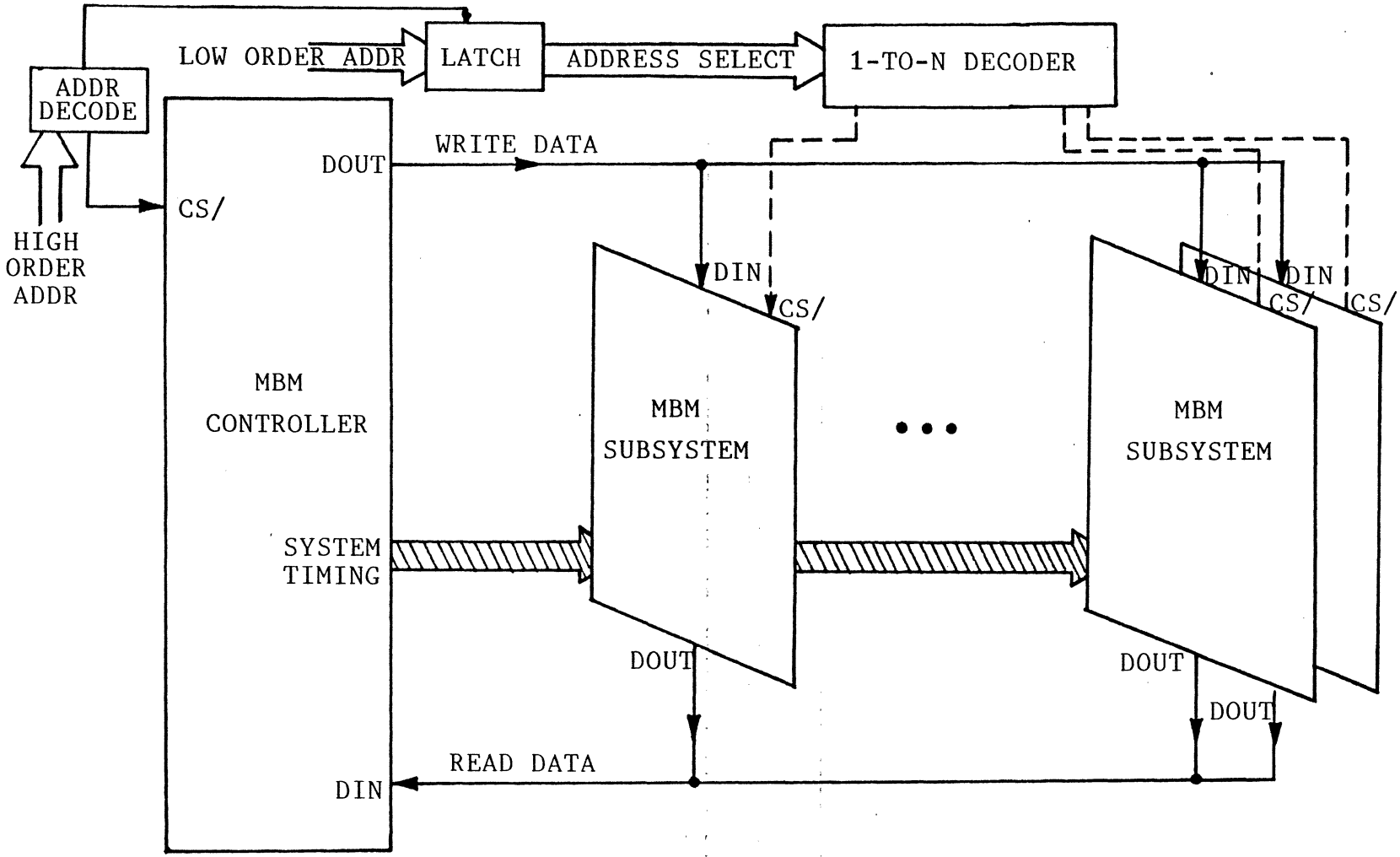


FIGURE 4.11

MULTIPLEXED OPERATION OF MBM SUBSYSTEMS

can be connected together and the need for shift registers is removed.

A multiplexed MBM system has the advantage of lower power dissipation for the same memory capacity because only one MBM subsystem is active at any time (equal to that of the minimum subsystem, when deselected subsystems are powered down). Also, the system can be expanded to any number of subsystems, only limited by the decoding circuitry provided.

The disadvantages of the multiplexed MBM system configuration, though, are the low data rate (same as the minimum system configuration) and longer average access times due to the overhead associated with switching from one subsystem to another, including initialization time.

The multiplexed MBM system component count is given in Table 4.5. A comparison of the average subsystem data transfer rate and average access time for parallel and multiplexed operation is given in Table 4.6.

4.4 HYBRID SYSTEM CONFIGURATIONS

Various combinations of the parallel-mode and multiplexed-mode of subsystem operation can be implemented to achieve the needs of the individual application. One popular example for large-capacity bubble memory systems would

MULTIPLEXED-MODE

MBM SYSTEM COMPONENT COUNT

256K and (1M)

TOTAL MEMORY CAPACITY (BYTES)	MBMs REQUIRED	SUPPORT CIRCUITS REQUIRED	CONTROL-LERS REQUIRED	MUX. DECODE AND SELECT LOGIC	TOTAL	AVE. Kbits PER PACKAGE
32K (128K)	1	5	1	0	7	36.6 (146)
64K (256K)	2	10	1	4	17	30.1 (120)
128K (512K)	4	20	1	4	29	35.3 (141)
256K (1M)	8	40	1	4	53	38.6 (151)

TABLE 4.5

MULTIPLEXED SYSTEM COMPONENT COUNT

256K (1M)

TOTAL MEMORY CAPACITY (BYTES)	PARALLEL-MODE		MULTIPLEXED-MODE	
	AVERAGE ACCESS TIME (mS)	BURST DATA RATE (Kbits/s)	AVERAGE ACCESS TIME (mS)	BURST DATA RATE (Kbits/s)
32K (128K)	6.9 (11.2)	125 (100)	$6.9+t_{sw}$ ($11.2t_{sw}$)	125 (100)
64K (256K)	6.9 (11.2)	250 (200)	$6.9+t_{sw}$ ($11.2t_{sw}$)	125 (100)
128K (512K)	6.9 (11.2)	500 (400)	$6.9+t_{sw}$ ($11.2t_{sw}$)	125 (100)
256K (1M)	6.9 (11.2)	1000 (800)	$6.9+t_{sw}$ ($11.2t_{sw}$)	125 (100)

*t_{sw} is the time to swtich from one MBM subsystem to another when required.

TABLE 4.6

PARALLEL- AND MULTIPLEXED-MODE COMPARISON

be the use of multiple MBM controllers with each controller operating eight bubble memory subsystems in parallel. In this particular configuration, the controllers are multiplexed, while the subsystems (of an individual controller) operate in parallel to obtain the maximum data transfer rate.

Parallel operation of MBM controllers could also be accomplished for systems with data paths wider than eight bits (e.g., 16- and 32-bit systems). An example of the hardware for this type of application is given in Figure 4.12.

For systems operating with the DMA data transfer mode, DRQ is formed by the AND of the individual controller DRQs, thus signalling that both controllers are ready for data or have data assembled. DACK/ is routed from the DMA controller to both DACK/s of the MBM controllers. In the interrupt-driven mode, either MBM controller INTR line will interrupt the host system, however, it is left to the interrupt service routine to ensure that DRQ (STR1) is set for both MBM controllers. When operating in the programmed-mode, the user must monitor the DRQ bits (STR1) of both MBM controllers and ensure that both are active prior to data transfer.

Special care must be taken when an error is detected by one of the MBM controllers in the transfer of data between

the MBM systems and the host system. This condition results in one MBM system halted while the other may be attempting to continue additional transfers. To prevent this hang-up mode, it is suggested that the ENABLE READY INTERRUPT option be selected. The detection of an error or the successful completion of commands will then interrupt the host system. The interrupt service routine should then poll the status registers of the MBM controllers to determine the nature of the interrupt and then act on it accordingly. In multiple page/sector transfers, with the STOP ON ERROR option selected, the two controllers could potentially come out of synchronization with each other. An initialize command to the MBM controller would act to re-synchronize the MBM systems with each other.

In selecting the MBM system configuration, it should be noted that parallel operation of MBM subsystems requires faster response times to a data request (DRQ) on the part of the CPU to prevent an overflow or underflow of the 16-byte data FIFO. Slow CPUs, therefore, may be unable to respond to DRQ fast enough for the MBM system. DMA controllers may be used, but in some applications, the additional hardware and software required may be too costly. A listing of the required response times to DRQ for 256K and 1Mbit MBM systems is given in Table 4.7.

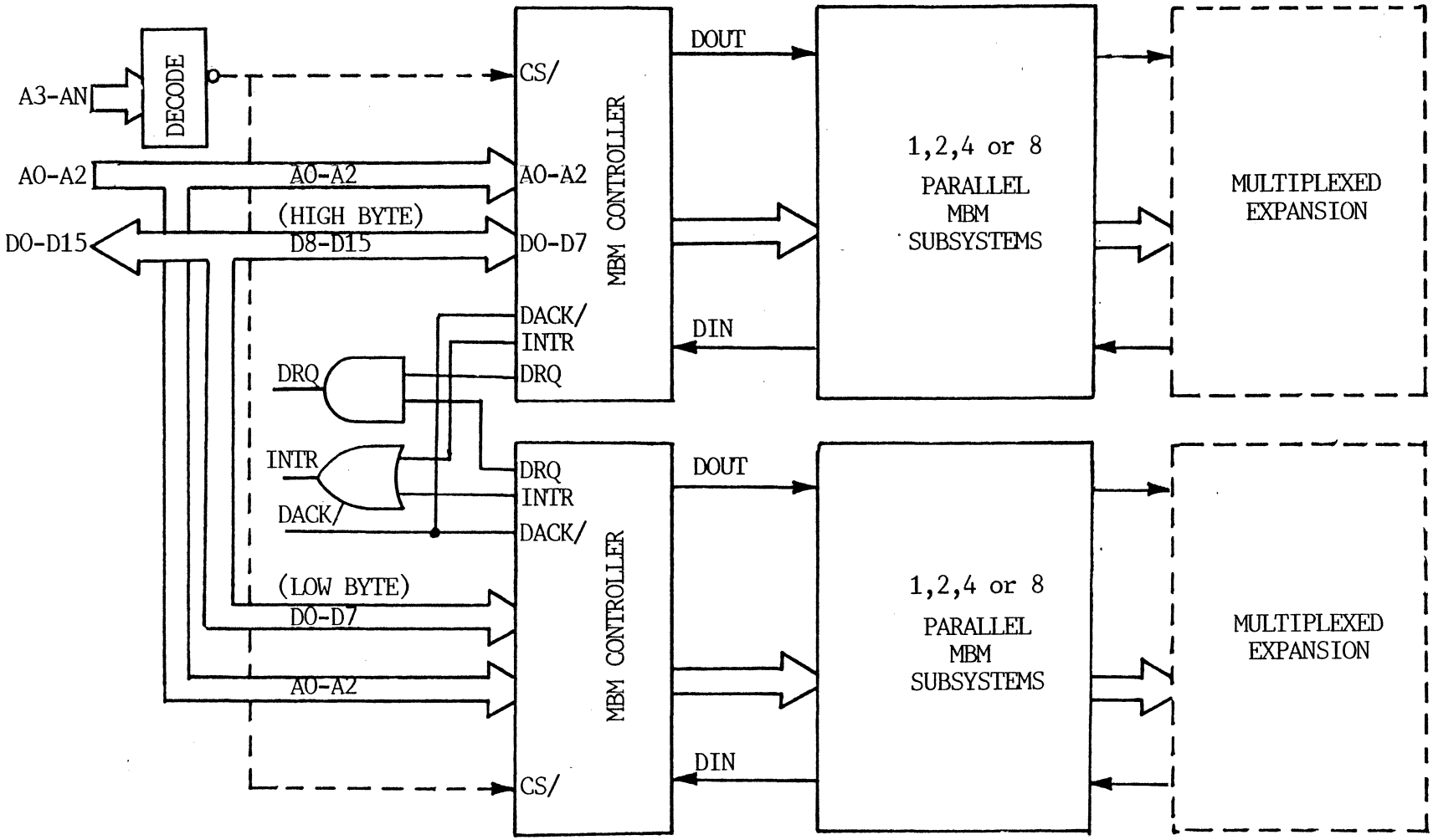


FIGURE 4.12

HYBRID MBM SYSTEM EXPANSION

256K (1M)

#MBMs IN PARALLEL	HALF BUFFER OPTION NOT SELECTED (μS)	HALF BUFFER OPTION SELECTED (μS)
1	1024 (1280)	512 (640)
2	512 (640)	256 (320)
4	256 (320)	128 (160)
8	128 (160)	64 (80)

TABLE 4.7

REQUIRED RESPONSE TIMES TO DRQ

CHAPTER 5

MBM SYSTEM PERFORMANCE ANALYSIS

The purpose of this chapter is to discuss the performance of the MBM system under actual operating conditions. The test hardware and software are briefly presented, followed by an evaluation of the support circuits, bubble memory, and controller performance. Overall system performance in the way of power dissipation and measured error rates is also discussed. The chapter then concludes with recommendations for extending the bubble memory operating range beyond 0 to 70° C.

5.1 TEST SYSTEM ARCHITECTURE

The hardware test system developed specially to test and exercise Motorola's 256K and 1Mbit bubble memory systems, support circuits and bubble memory devices is depicted in Figure 5.1. It consists of a 4MHz M6809 microprocessor-based development system with a CRT display, ASCII keyboard, floppy disk drive and a minimum of 32 KBytes of RAM. The bubble memory interface and bubble memory subsystem are interfaced directly to the M6809 system data bus and address bus. Provisions for monitoring the hardware operations

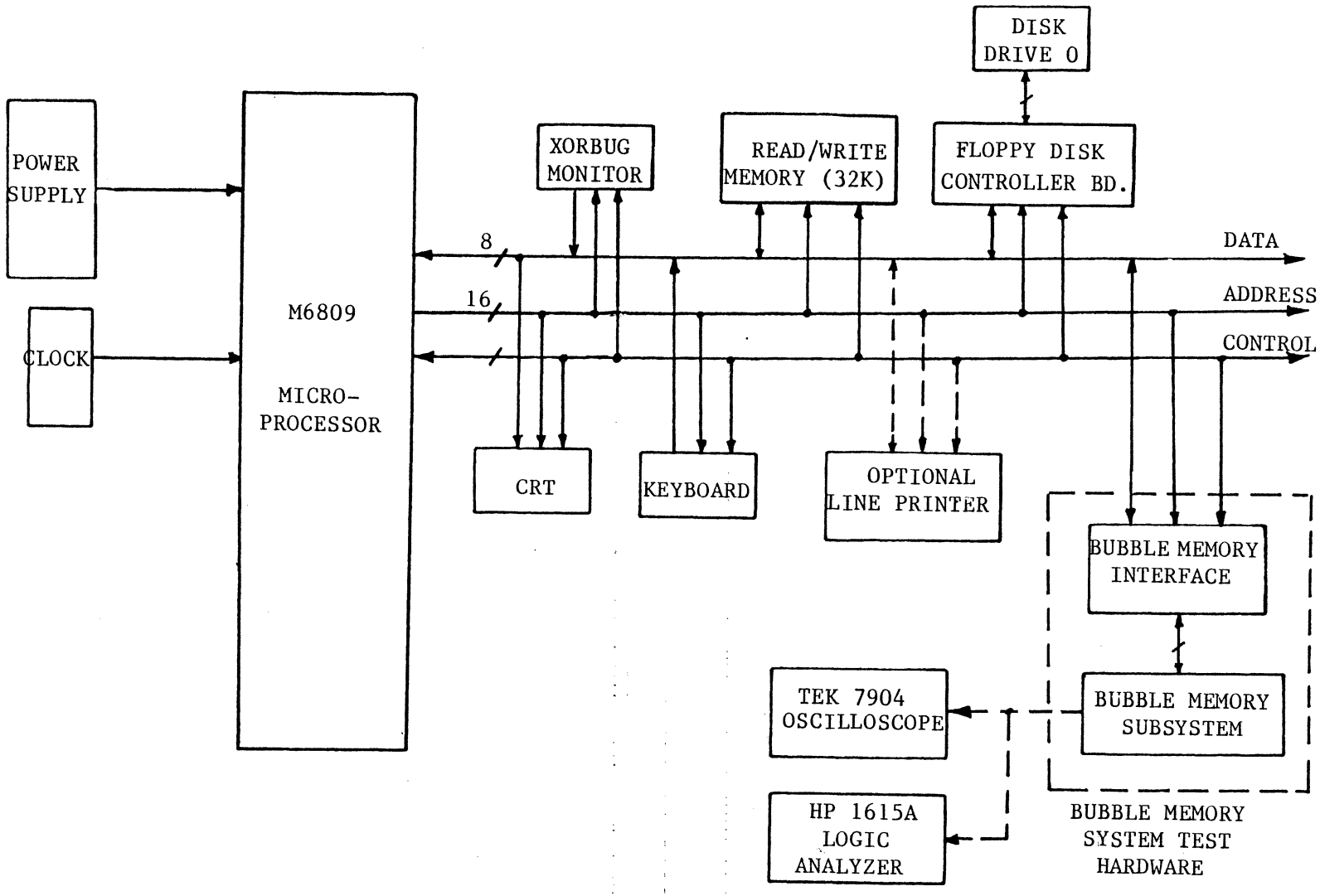


FIGURE 5.1

BUBBLE MEMORY TEST SYSTEM HARDWARE

of the MBM system are made possible with test points and current loops.

The bubble memory system test hardware is designed such that it can be configured remote from the main tester hardware. This makes the MBM test system suitable for testing in environmental and temperature chambers.

BUBLTEST is a bubble memory diagnostic test software package developed specially to control and exercise the bubble memory system and to monitor the performance of the overall system as well as the individual components of the MBM system. Figure 5.2 shows the general structure of the BUBLTEST software and its menu-driven approach. The user has various options available to him that allow for conducting everything from single-step operations on up through long-term life tests. A more detailed description of BUBLTEST is given in the reference manual in Appendix A.

5.2 MBM SYSTEM PERFORMANCE

Chapter 1 and Chapter 2 discussed the strict operational requirements of the bubble memory device. The purpose of this section is to discuss the resulting performance of the components of the MBM system with respect to the ideal requirements pointed out in those earlier chapters.

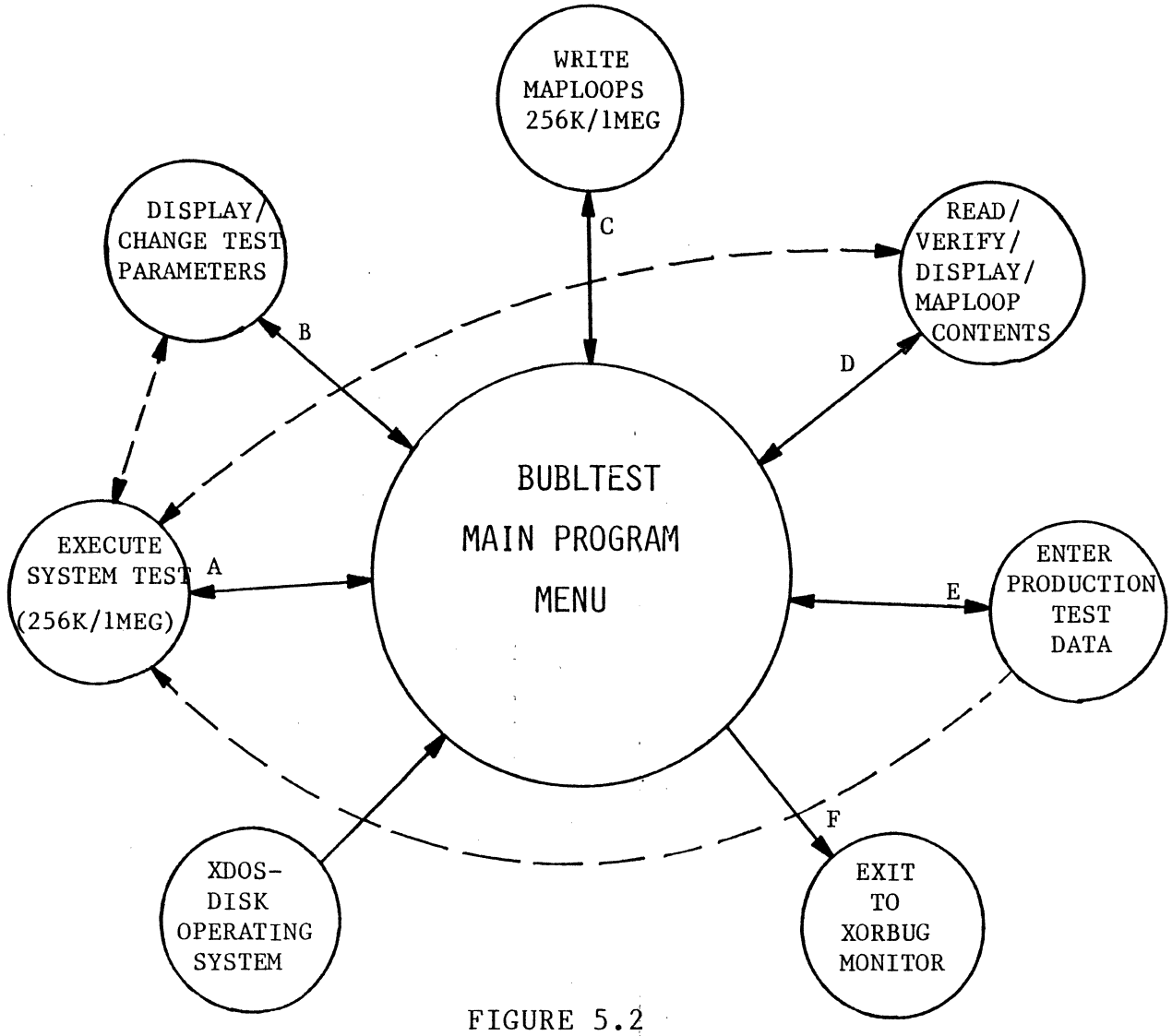


FIGURE 5.2

BUBBLE MEMORY TEST SYSTEM SOFTWARE

The performance of the 1Mbit system is presented here. The 256Kbit performance can be described as comparable.

It was pointed out in Chapter 2 that the coil drive currents used for propagation of bubble domains within the magnetic film material and along the tracks established by the nickel-iron chevrons were required to be a certain peak amplitude and also to start-up and shut-down in a certain sequence.

The optimum coil drive peak amplitudes are specified in the bubble memory specification as I_X = 650mA and I_Y = 740mA. Measured coil currents in the MBM system are I_X = 700mA and I_Y = 780mA. This represents less than a 10% increase in drive currents, however, as seen in Figure 2.3, this increase puts the MBM device further into its operating region. The undesirable effect of these increased coil currents is that the device will dissipate slightly more power.

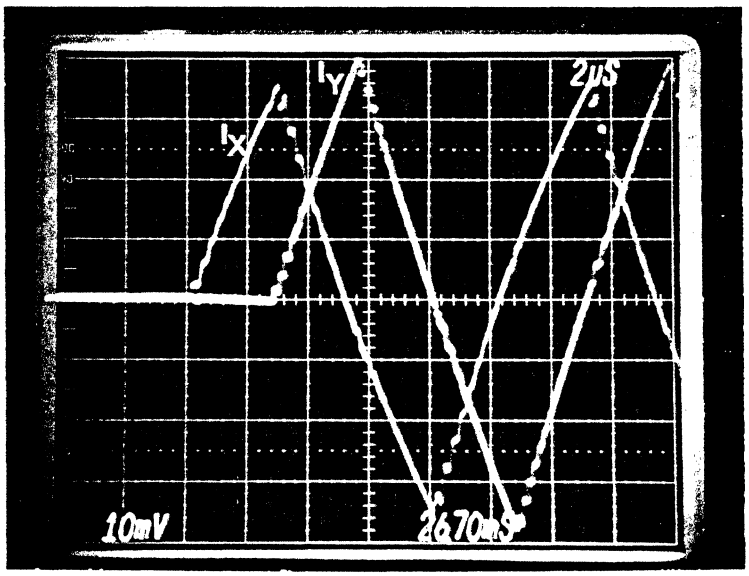
The start-up coil currents are near ideal. The X coil current starts approximately 90 degrees before the Y coil current. The coil shut-down sequence takes place smoothly also. In order to avoid current overshoots which could distrub stable bubble positions during the stop cycle, though, the currents are allowed to exponentially decay once they are near zero current. This changes the drive field vector slightly, but this has not been found to in

any way affect performance. Figure 5.3 shows the coil current start-up and shut-down cycles. Figure 5.4 shows the MBM propagation cycle and also the coil current vector representation.

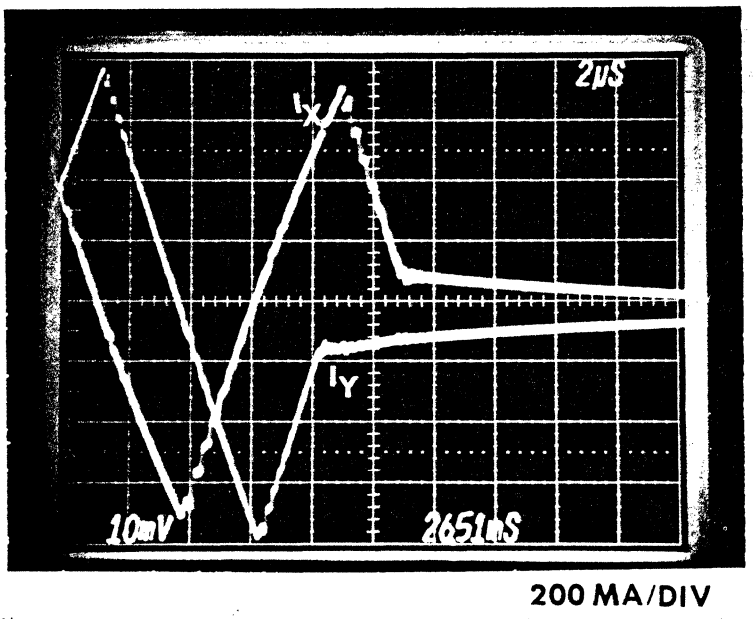
The slight phase shift noted in Figure 5.4(b) is the result of the X and Y coil currents not being exactly 90 degrees out of phase with each other. This phase shift in the resultant drive field is accounted for, though, by the MBM controller timing generator which delays the function current timing pulses and also takes the support circuit delays into account.

Photographs of the function currents are given in Figures 5.5 through 5.8. Optimal function current amplitudes are obtained when a 6.19 Kohm (±1%) set resistance is used. As required, the cut currents (i.e., I_{RC} and I_{MC}) have fast rise and fall times to facilitate the splitting of bubble domains at the replicator gates. On the other hand, the generate fall time is controlled to be slow to prevent the multiple nucleation of bubble domains.

Finally, Figure 5.9 shows the resulting differential detector output voltage of the bubble memory active and reference detector elements. The signal shown is particularly small in amplitude (approximately 10mV of margin between the one and zero signal), but illustrates the ability



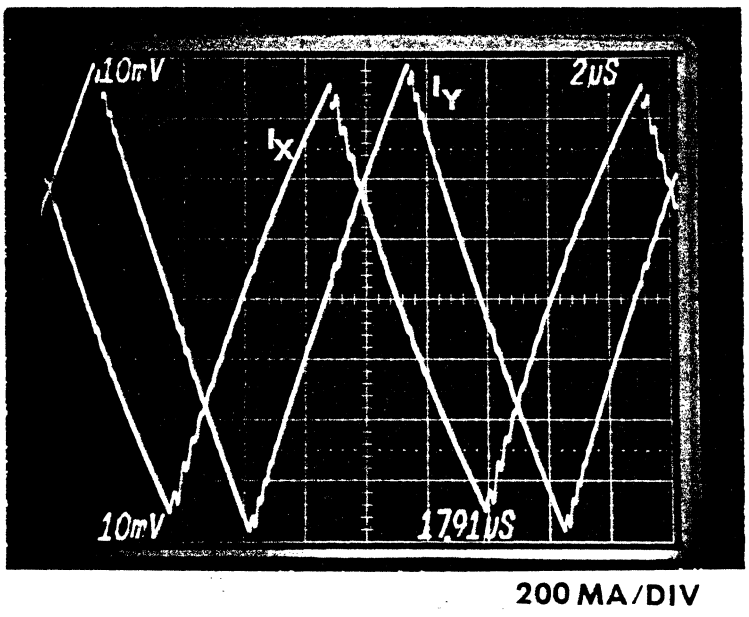
(a) COIL CURRENT START-UP CYCLE



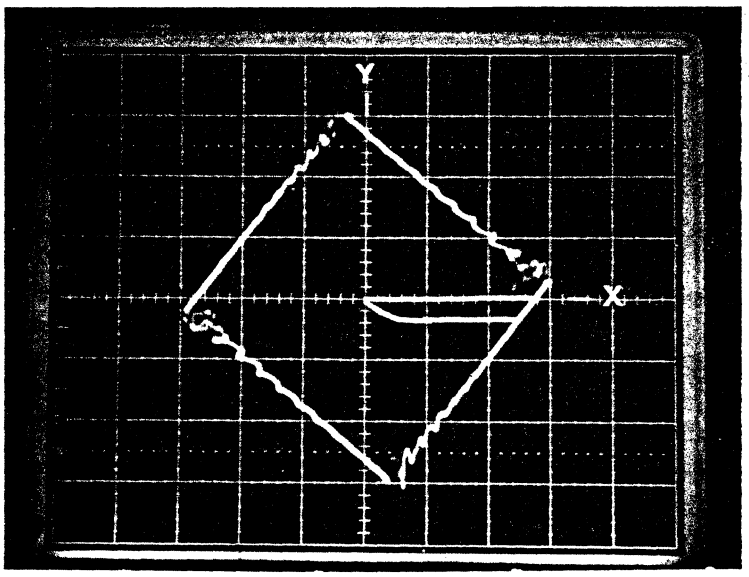
(b) COIL CURRENT SHUT-DOWN CYCLE

FIGURE 5.3

COIL CURRENT START-UP AND SHUT-DOWN CYCLES



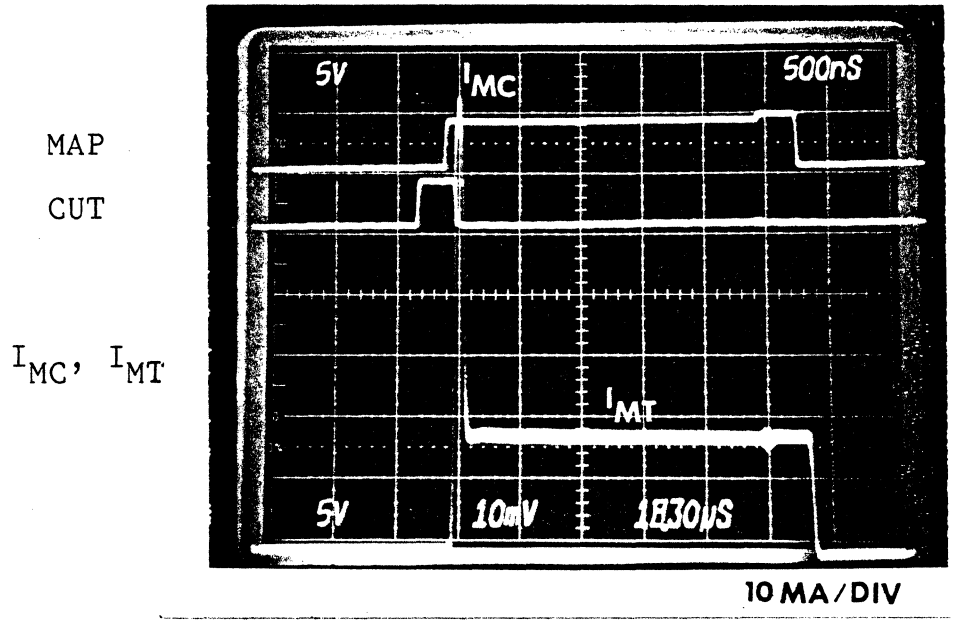
(a) MBM PROPAGATION CYCLE



(b) DRIVE FIELD VECTOR

FIGURE 5.4

COIL CURRENT RUN CYCLE AND VECTOR REPRESENTATION



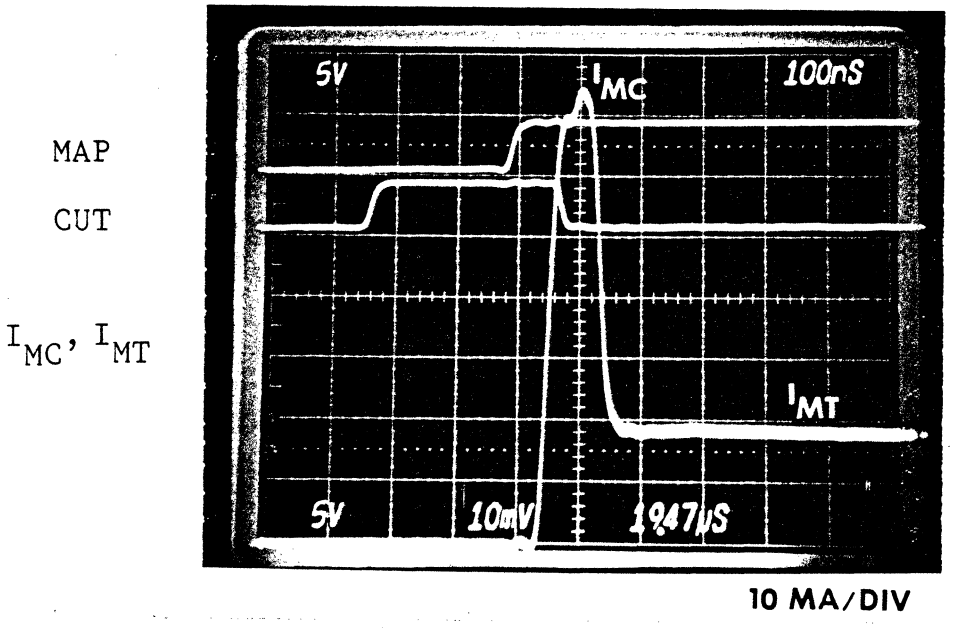


FIGURE 5.5

MAP REPLICATE-CUT AND TRANSFER-OUT CURRENTS

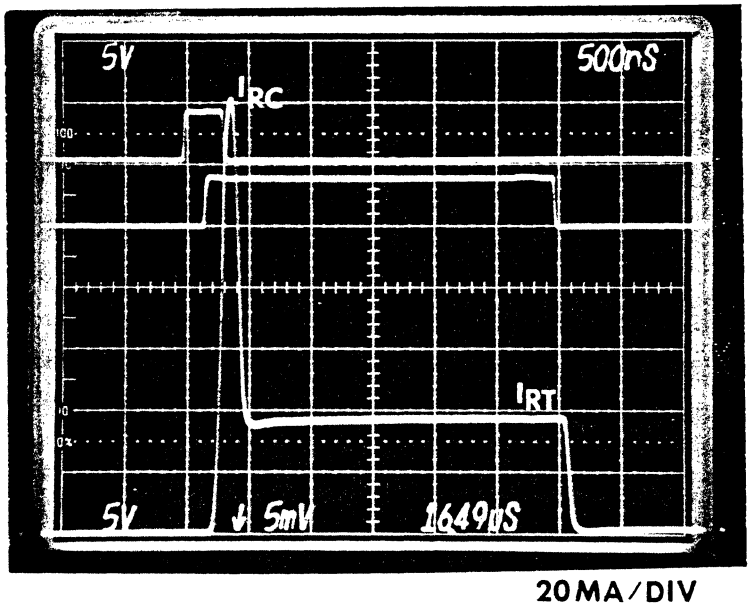


FIGURE 5.6

DATA REPLICATE-CUT AND TRANSFER-OUT CURRENTS

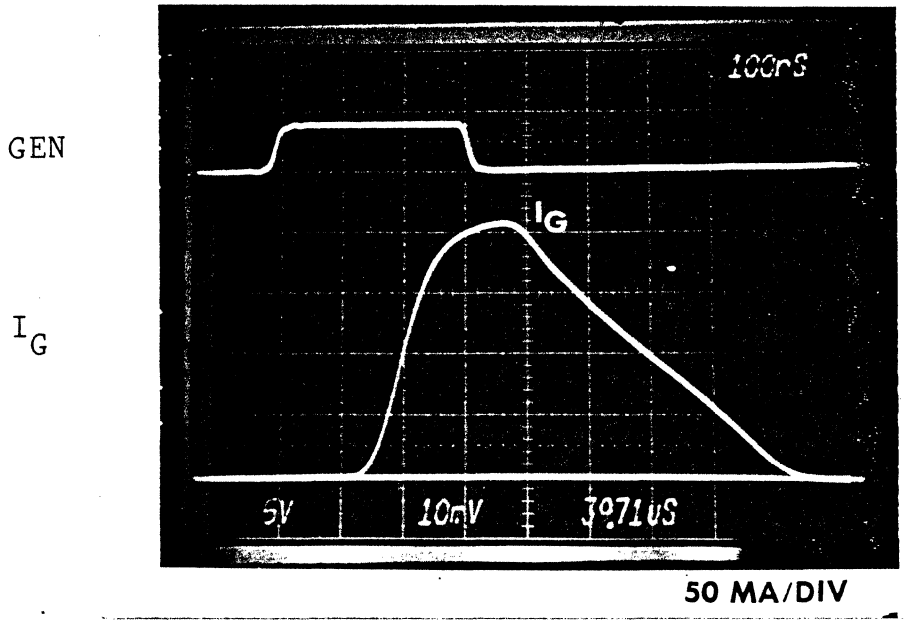


FIGURE 5.7

GENERATE CURRENT

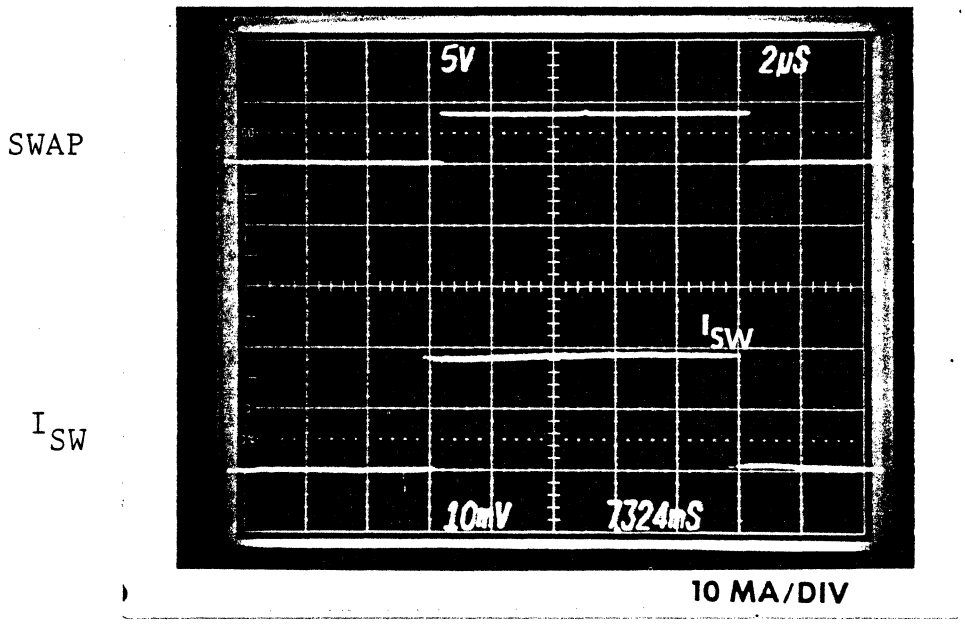
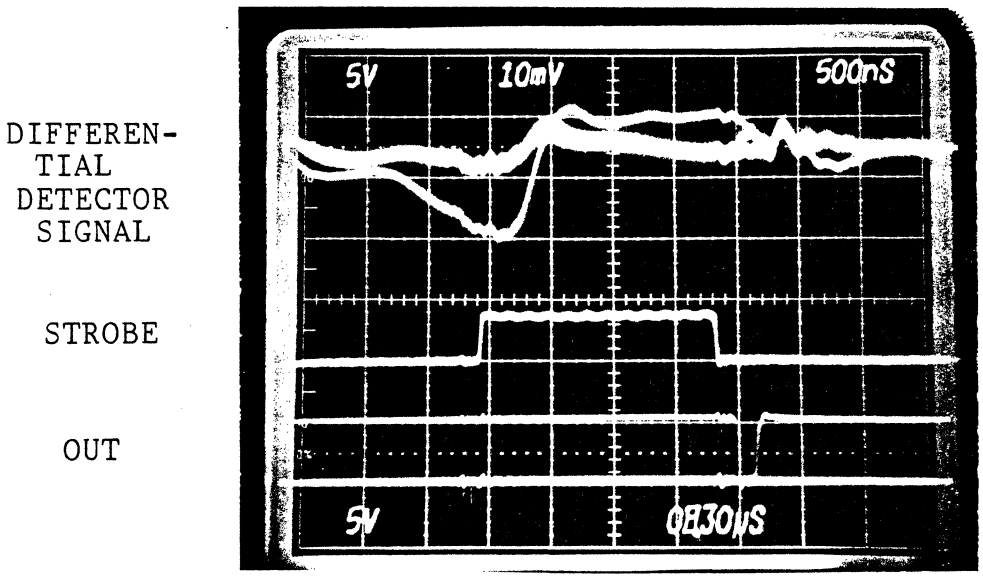


FIGURE 5.8

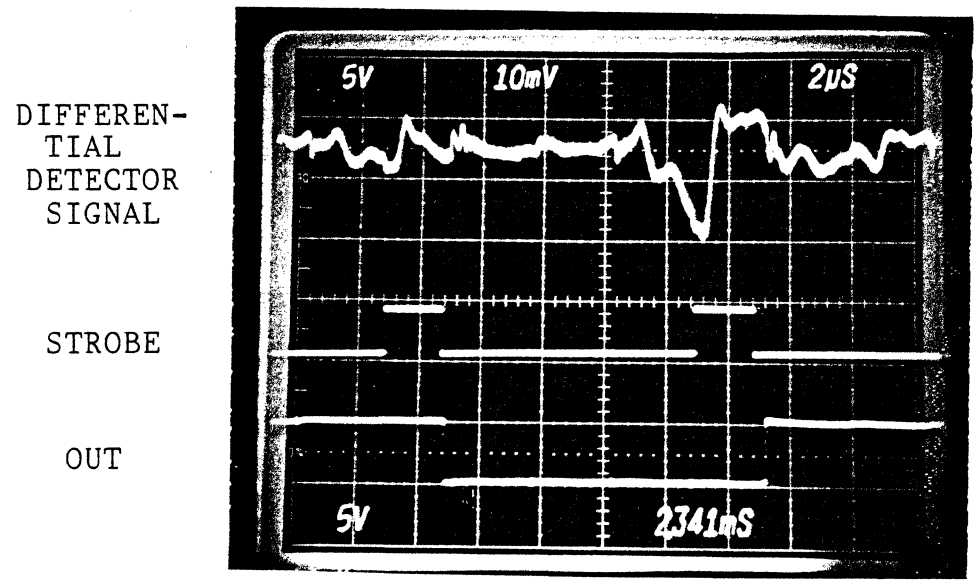
DATA SWAP CURRENT

of the MBM Sense Amplifier to distinguish between the one and zero signals.

As discussed in earlier chapters, the MBM detector signal output voltages vary over temperature. At high temperatures, the one and zero signals decrease in amplitude, although not at the same rate. At low temperatures, the one and zero signals increase in amplitude, again at different rates. Using the nominal MBM Sense Amplifier threshold of 14mV will result in reliable operation from 0 to 70° C with most MBM devices. However, to improve signal-to-noise margin and subsequently, overall system reliability, it is recommended that the MBM Sense Amplifier threshold be temperature compensated. This compensation is required if operation outside 0-70°C is to be obtained. Figure 5.10 illustrates the variation in detector signal amplitudes and the threshold compensation recommended. To obtain this compensation, the network of Figure 5.11 is used. Note that the positive temperature coefficient thermistor does not compensate nearly as much as the negative temperature coefficient thermistor, however, it does add a bit more margin. In applications where system cost is of great concern, this thermistor can be eliminated, and a 3.3Kohm, 1% film resistor used in its place.



(a) SUPERIMPOSED SIGNALS



(b) SERIAL DATA SIGNALS

FIGURE 5.9

BUBBLE MEMORY DETECTOR SIGNALS

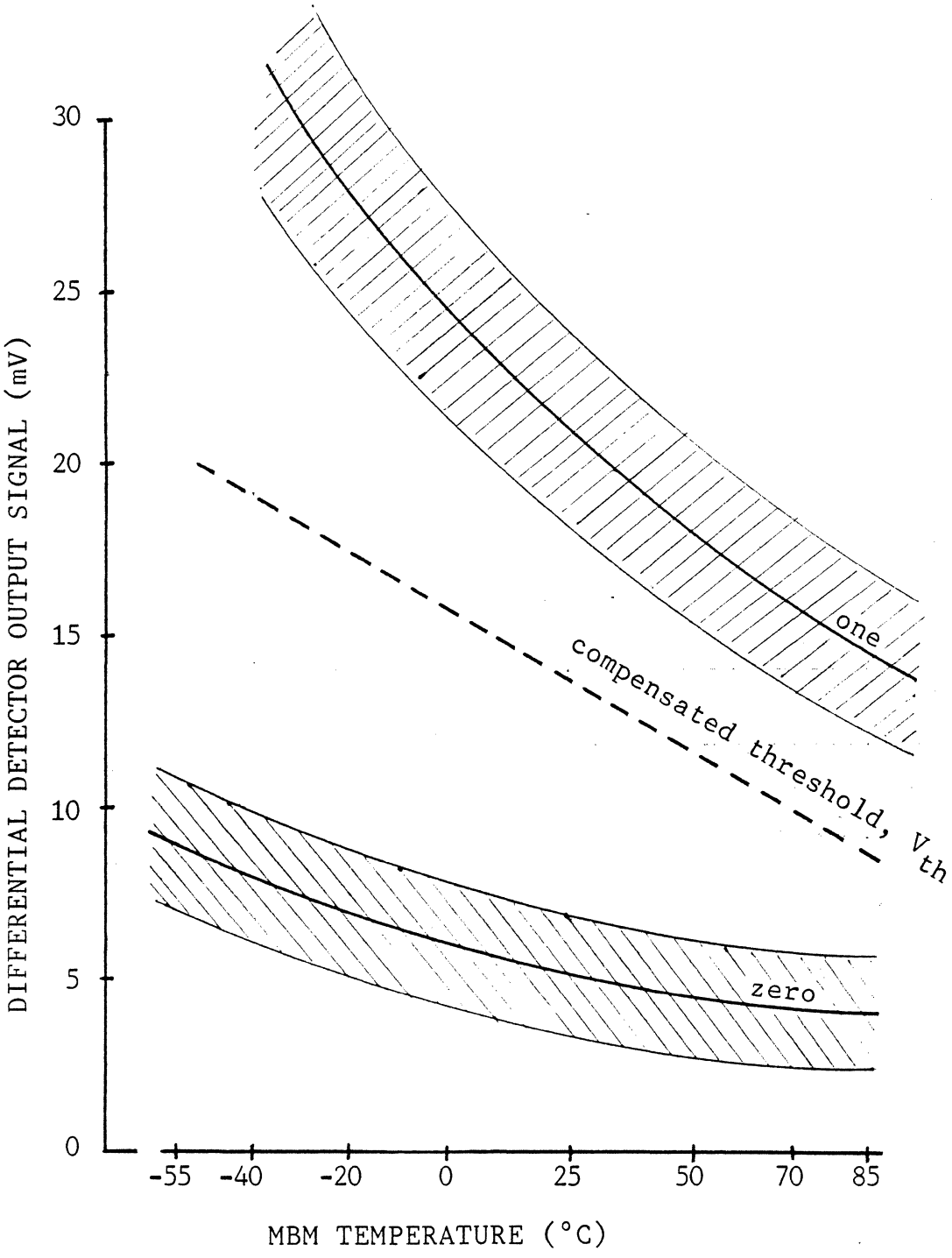


FIGURE 5.10

MBM DETECTOR SIGNAL THRESHOLD COMPENSATION

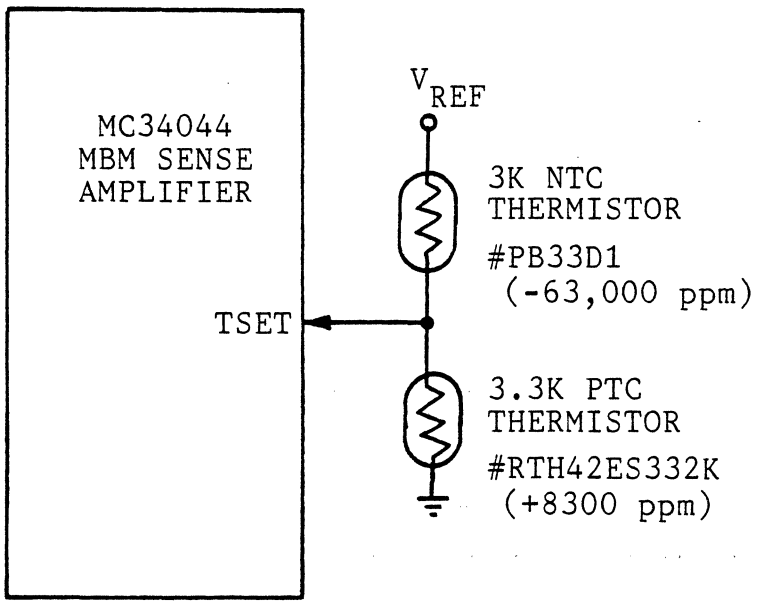


FIGURE 5.11

MBM DETECTOR SIGNAL THRESHOLD COMPENSATION NETWORK

5.3 MBM SYSTEM POWER DISSIPATION

The measurements of the MBM system typical power dissipations over temperature are listed in Table 5.1. Note that the single one megabit (128 KBytes) MBM system typically dissipates less than 2 watts of power in the standby mode in the temperature range of 0 to 70° C. (Naturally, since the bubble memory is a non-volatile storage device, the entire MBM system can be powered-down between accesses, if necessary, to reduce power drain to zero.) Also note that the typical active power dissipation within the 0 to 70° C temperature range is less than 4 watts.

Table 5.2 lists the typical power dissipation for the individual components of the MBM system as measured at 0° C.

5.4 MBM SYSTEM ERROR RATES

MBM system error rates are, in general, a good measure of the overall system performance primarily for two reasons: (1) they serve as a measure of the quality of the system hardware and (2) they are a means of determining the adaptability of the bubble memory system to high-reliability applications. The types of errors observed in bubble memories and their potential causes are discussed in Section 3.2.4.

POWER (WATTS)

SUPPLY	T= -40°C		T= 0°C		T= 25°C		T= 70°C		T= 85°C	
	STANDBY	ACTIVE	STANDBY	ACTIVE	STANDBY	ACTIVE	STANDBY	ACTIVE	STANDBY	ACTIVE
+12V	0.88	2.48	0.78	2.60	0.68	2.60	0.64	2.67	0.62	2.65
+5V	1.26	1.26	1.10	1.12	0.99	1.00	0.92	0.93	0.89	0.90
TOTAL	2.14	3.74	1.88	3.72	1.67	3.60	1.56	3.60	1.51	3.55

Note: Single one megabit MBM system in the minimum system configuration.
Active power dissipation is measured at 100% duty cycle.

TABLE 5.1

TYPICAL MBM SYSTEM POWER DISSIPATION

TYPICAL POWER (WATTS)

MBM COMPONENT	STANDBY	ACTIVE
SC42585 MBM CONTROLLER	0.57	0.58
MC34044 MBM SENSE AMP.	0.21	0.21
MC34047 MBM OP DRIVER	0.41	0.41
SC42468 MBM COIL PREDRIVER	0.55	0.60
MTQ5NP03 MBM COIL PREDRIVER	0	1.90
MBM2011 MBM DEVICE	0.10	0.10

Note: Measured at 0° C
Active measurements at 100% duty cycle.

TABLE 5.2

MBM SYSTEM COMPONENT POWER DISSIPATION

Determination of error rates in bubble memory systems is, in general, a bilateral determination; that is, the hard error rate and the soft error rate. Since soft errors are related to the bubble detection operation, they can be expressed as the number of errors per bit read. However, hard errors are related to the actual MBM write operation and also to the propagation characteristics of the MBM drive field. In the former case, it would make sense to express the hard error rate as the number of errors per bits written, while the latter case suggests that it be expressed as the number of errors per MBM propagation cycle.

Regardless of the method used to express the error rate of the bubble memory system, the error rates have been determined to be extremely small and therefore, are very difficult to measure. Despite this, an attempt to actually measure the error rate and avoid the extrapolation of incomplete results has been made.

The hardware test system and software described in Section 5.1 were used, along with a temperature chamber, to document MBM system performance based on error rates. A temperature chamber was temperature-cycled from 0 to 70° C with several MBM system boards exercised within. Some systems were also run from -40 to 85° C, although this data comprised the minority of the recorded data.

The test run starts with 50 system initializations and 2 map reads separated by another system initialization. Both constant data patterns and randomly-generated data were then written to the bubble memory system to its capacity. The entire memory was then read twice, with all errors being recorded and documented on a line printer. All data patterns and random seeds were then changed and the test repeated again. Errors in the ECC bits were also checked for. Table 5.3 lists the characteristics of each test run (one full memory write followed by two full memory reads).

Table 5.4 lists the results of the error rate testing conducted on 20 one megabit bubble memory systems for a period of many months. One multiple-device MBM system (2-device) was used in the testing as well as 18 minimum system configurations.

As shown, no soft errors were encountered throughout the duration of the complete testing. This corresponds to a soft bit error rate of approximately 5×10^{-12} with a relatively weak degree of certainty. Estimating this error rate to be approximately 5×10^{-11} improves the degree of certainty to approximately 99 percent.

ERROR RATE TEST CHARACTERISTICS PER TEST RUN

# MBM PROPAGATION CYCLES	=	12,204,087
# COIL START AND STOPS	=	6,199
# PAGE WRITES (i.e., # SWAPS)	=	2,048
# PAGE READS (i.e., # DATA REPLICATES)	=	4,096
# MAP BIT READS (i.e., # MAP REPLICATES)	=	42,821
# DATA AND ECC BITS WRITTEN	=	1,073,152
# DATA AND ECC BITS READ	=	2,146,304

TABLE 5.3

ERROR RATE TEST CHARACTERISTICS

ERROR RATE PERFORMANCE DATA

MBM DEVICES USED	= MBM 2011
NUMBER OF MBMs TESTED	= 20
TOTAL NUMBER OF TEST RUNS	= 90,926
TOTAL BITS WRITTEN	= 9.8×10^{10}
TOTAL BITS READ	= 2.0×10^{11}
TOTAL MBM PROPAGATION CYCLES	= 1.1×10^{12}
TOTAL NUMBER OF SOFT ERRORS	= 0
MEAN SOFT ERROR RATE	$\leq 5.0 \times 10^{-12}$
TOTAL NUMBER OF HARD ERRORS	= 11
MEAN HARD ERROR RATE (BASED ON BITS WRITTEN)	= 1.1×10^{-10}
MEAN HARD ERROR RATE (BASED ON MBM PROPAGATION CYCLES)	= 1.0×10^{-11}

TABLE 5.4

ERROR RATE TESTING RESULTS

The total number of documented hard errors, on the other hand, was 11 for the duration of the testing. It should be noted here that all hard errors observed were found during the first read of that particular page in error. This suggests that the hard errors most likely occurred during the actual write operation, rather than due to propagation faults. Thus, the measured hard error rate can be expressed as the number of errors per bit written and is therefore 1.1×10^{-10}.

5.5 WIDE TEMPERATURE OPERATION

Extending MBM system operation beyond the 0 to 70° C temperature range requires a variety of compensation schemes for the sensing threshold, function current amplitudes, bias field intensity, and drive field intensity.

As discussed in Section 5.2, the MBM detector output signal varies over temperature. To maintain the maximum signal-to-noise margin the temperature compensation circuit of Figure 5.11 can be implemented.

Likewise, in wide temperature applications, the peak current amplitudes of some of the function currents must be made to track the MBM case temperature. Empirical data collected over many bubble memory devices clearly suggests that the transfer-out and swap currents need not be compensated over wide temperature ranges (-55 to

85° C). The generate, data replicate-cut and map replicate-cut, however, must be compensated as shown in the graph of Figure 5.12. This temperature compensation can be easily accommodated using the circuit of Figure 5.13.

Figure 5.14 shows the variation in bias field margin as a function of the MBM temperature. Clearly, the graph suggests the sufficient operating margin is available in the 0 to 70° C temperature range. However, outside that temperature range, the margin degrades significantly. Thus, temperature compensation of the bias field by applying a DC current through the Z coil in the reverse direction would result in maintaining a reasonable bias margin at temperatures beyond 0 to 70° C. The Z coil current required at various temperatures is plotted in the graph of Figure 5.15.

Finally, since bubble domains become somewhat sluggish in their movements at low temperatures, the drive field must be compensated to produce an increased drive field at low temperatures. This can be easily accommodated using a variable power supply and adjusting the V_{COIL} voltage to that shown in the graph of Figure 5.16 for the particular MBM temperature.

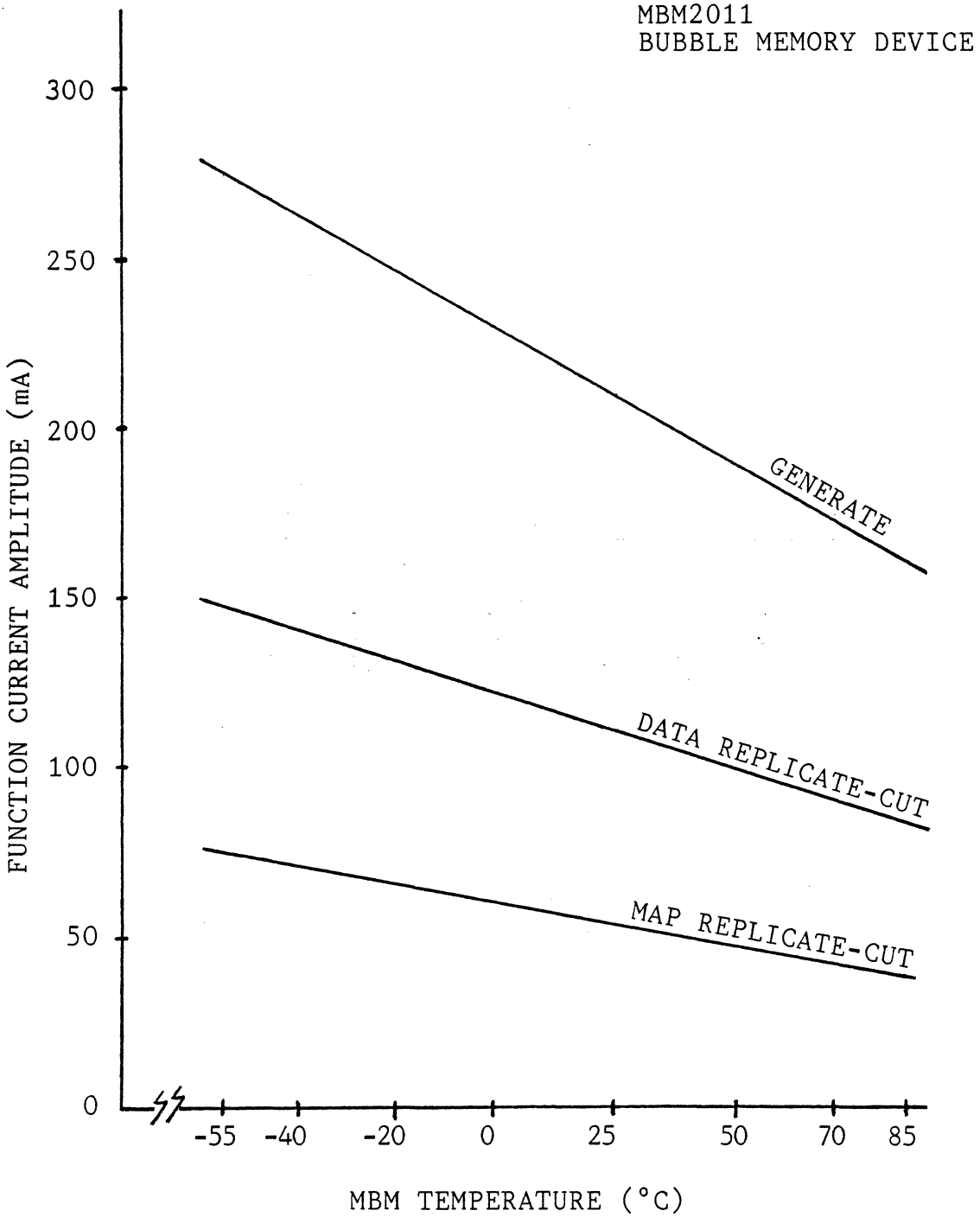


FIGURE 5.12

FUNCTION CURRENT TEMPERATURE COMPENSATION

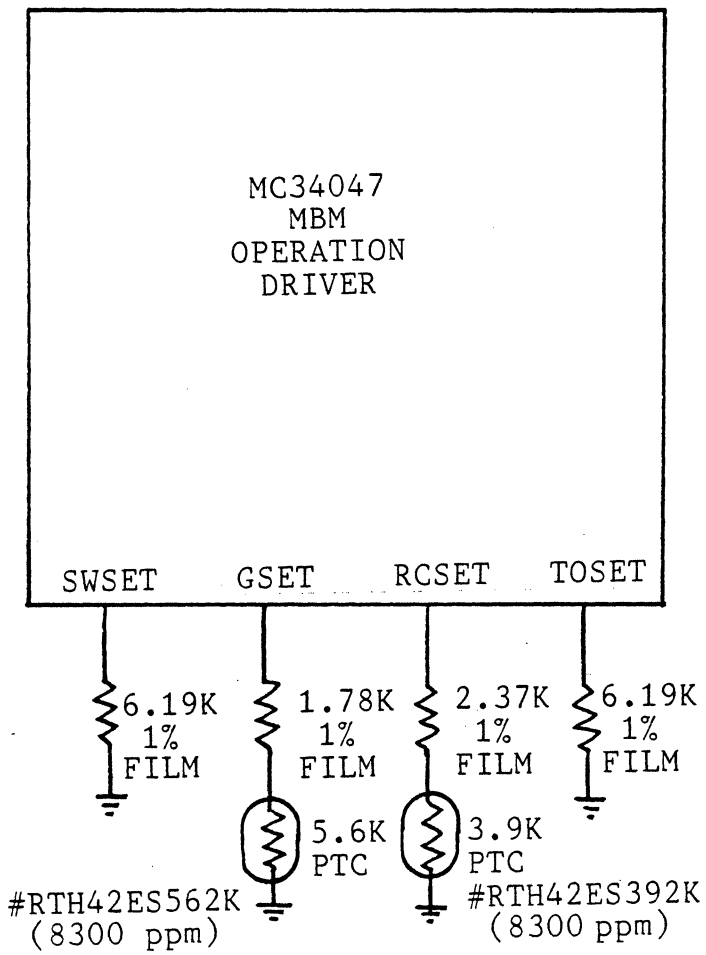


FIGURE 5.13

FUNCTION CURRENT COMPENSATION USING THE MC34047

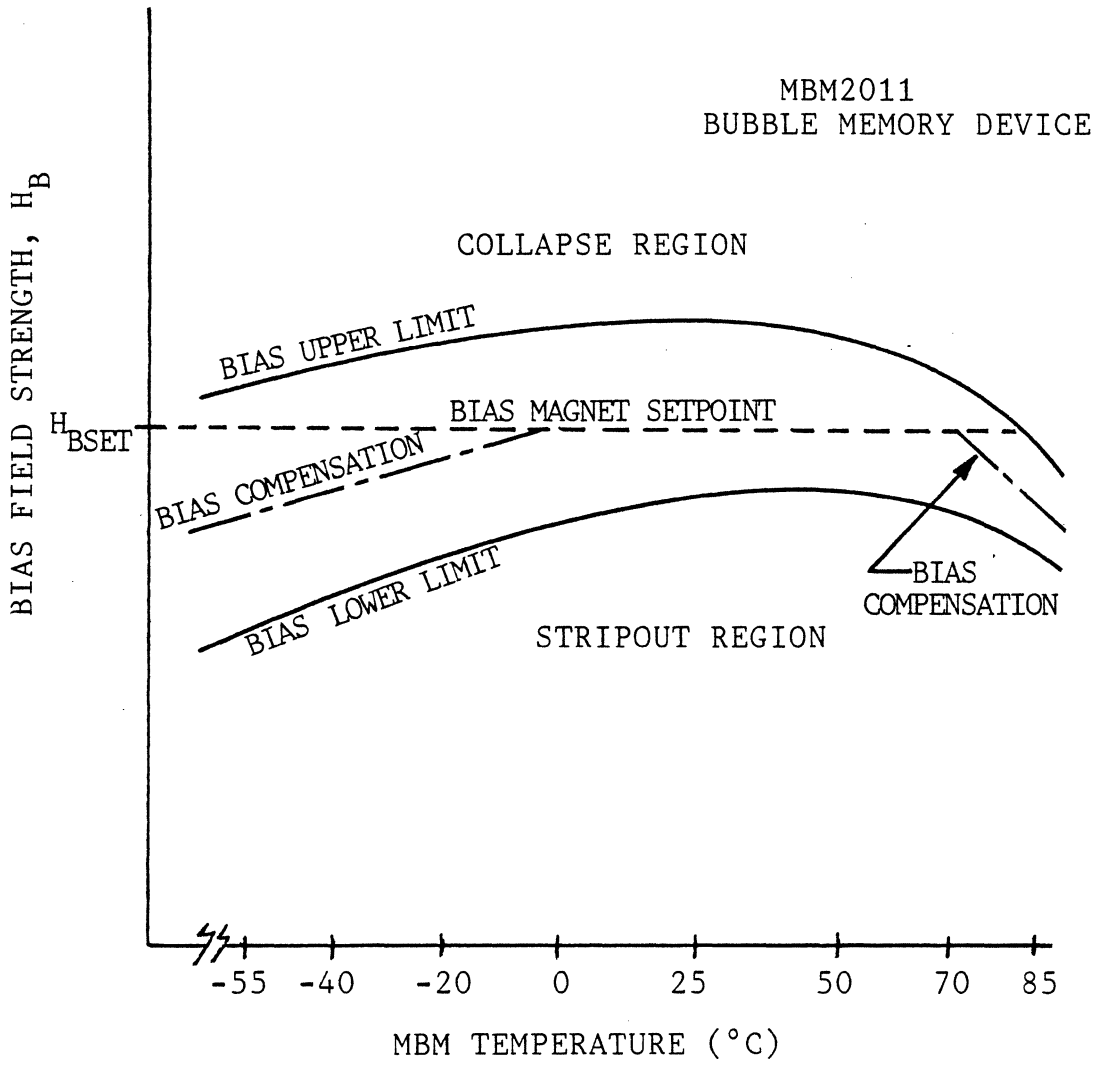


FIGURE 5.14

BIAS FIELD TEMPERATURE COMPENSATION

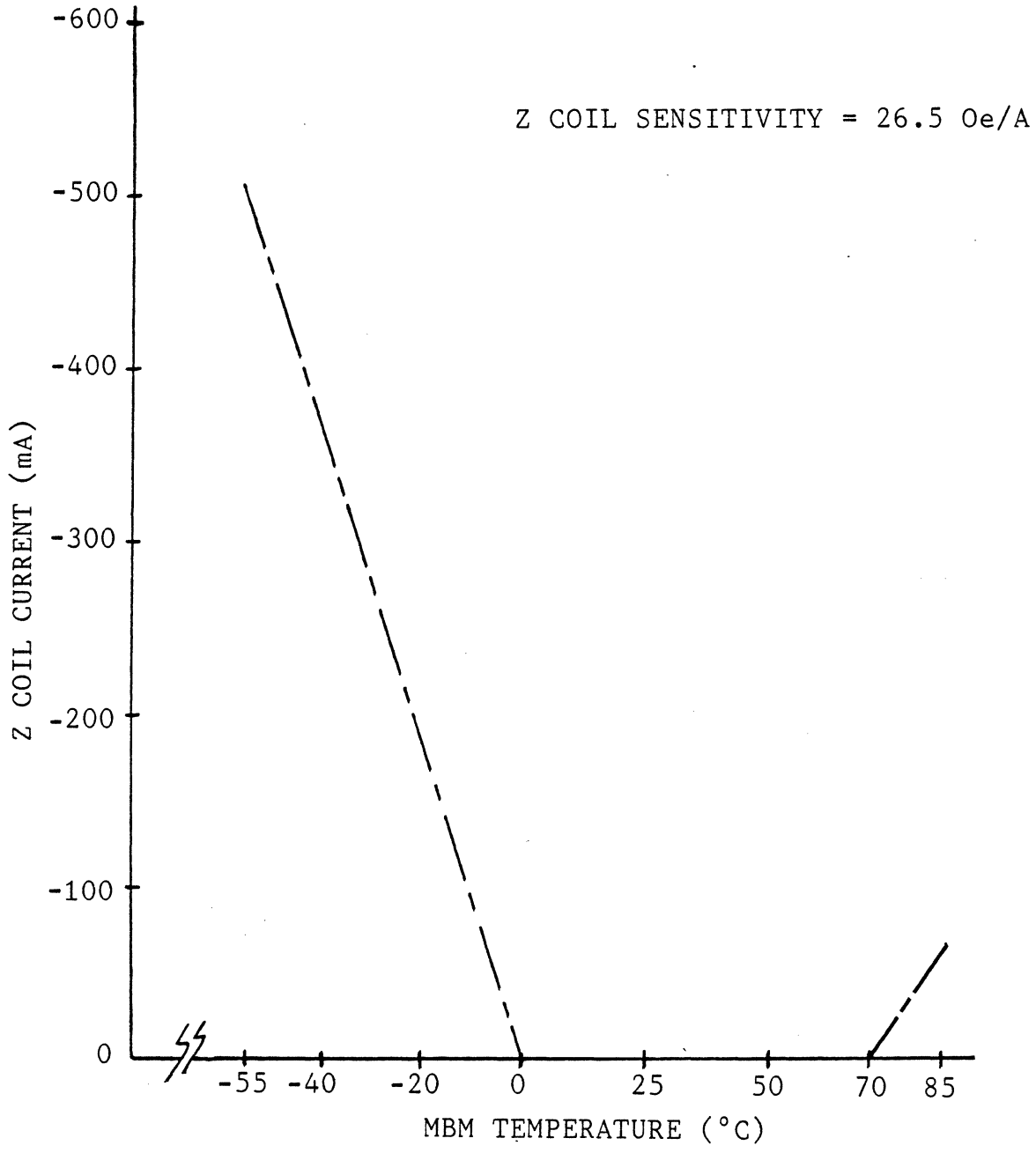


FIGURE 5.15

BIAS FIELD COMPENSATION USING THE Z COIL

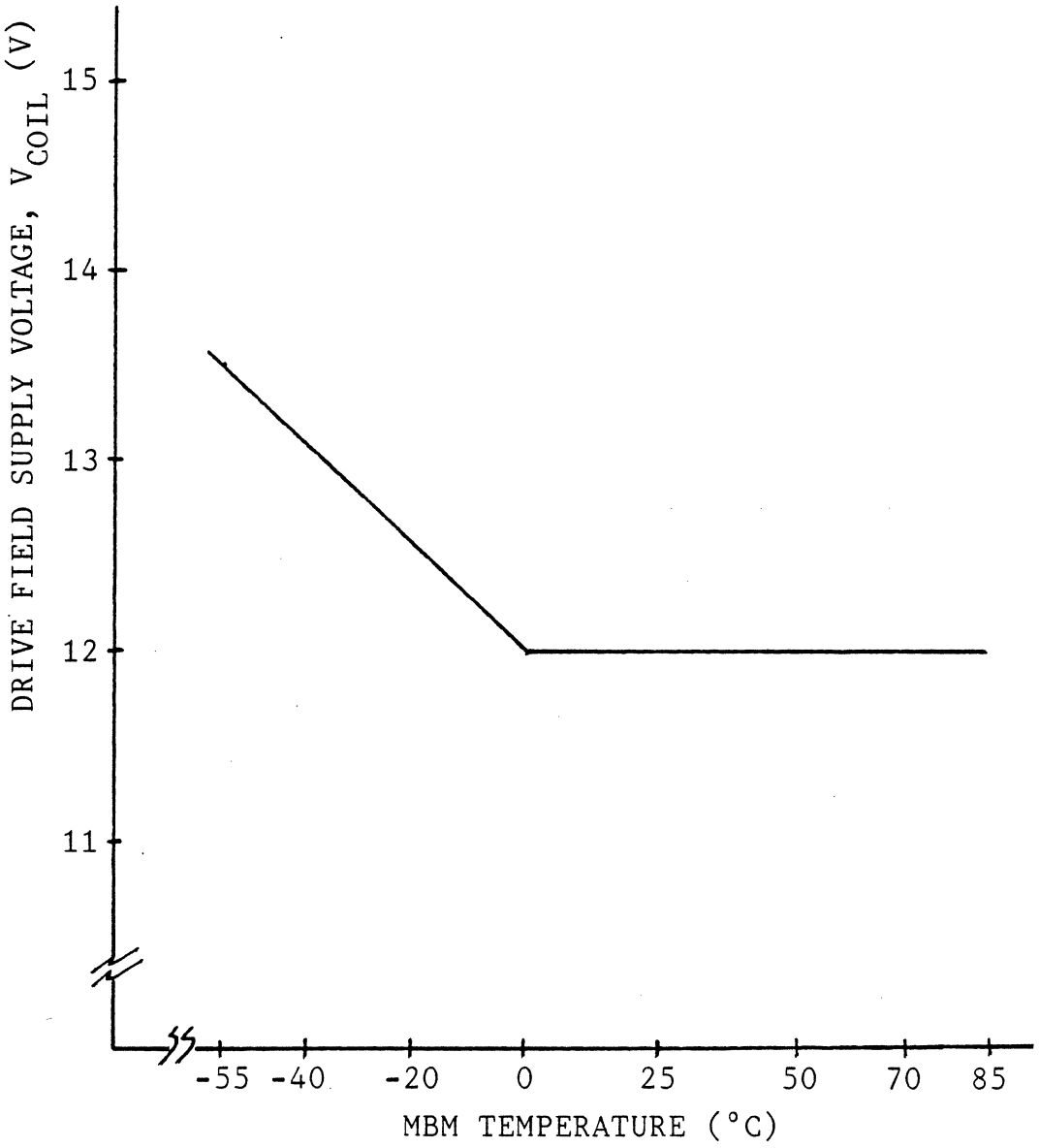


FIGURE 5.16

DRIVE FIELD COMPENSATION BY CHANGING V_{COIL}

CHAPTER 6

COMPARATIVE SYSTEM PERFORMANCE

The purpose of this chapter is to discuss the performance characteristics of Motorola's one megabit bubble memory system and compare it with that of other currently available bubble memory systems having the same user memory capacity. Also discussed is the performance characteristics of bubble memory systems in relation to other types of storage media. The chapter concludes with some generalizations regarding potential application areas for bubble memories.

6.1 THE COMPETITION

Four major manufacturers remain in the world market for the production of magnetic bubble memory devices. They are Motorola, Intel, Hitachi and Fujitsu. Table 6.1 is a comparison of the one megabit MBM system products of each of these major manufacturers.

Some interesting characteristics of these MBM systems are worth mentioning here. The Intel and Hitachi bubble memory devices have very long storage loops (4096 bits each). This results in long access times and long loop

PERFORMANCE CHARACTERISTIC	MOTOROLA MBM2011EK	INTEL BPK 72	HITACHI BEL0832A	FUJITSU FBE501M4E
MEMORY DEVICE #	MBM2011A	7110A	BDL0133	FBM54DB
MEMORY CAPACITY (KBYTES)	128	128	128	128
MEMORY ARCHITECTURE	BLOCK SWAP/ REPLICATE	BLOCK SWAP/ REPLICATE	BLOCK SWAP/ REPLICATE	BLOCK SWAP/ REPLICATE
MINOR LOOP LENGTH	2048	4096	4096	2048
NUMBER OF PAGES	2048	2048	4096	2048
# BYTES / PAGE	64	64	32	64
DRIVE FIELD FREQUENCY (KHz)	100	50	100	100
LOOP CYCLE TIME (mS)	20.5	81.9	41.0	20.5
MAX. TRANSFER RATE (KB/s)	12.5	12.5	12.5	12.5
SUPPLY REQUIREMENTS	+5V @.30A	+5V @.39A	+5V @.70A	+5V @.50A
	+12V @.35A	+12V @.40A	+24V @.30A	+12V @.04A
				-12V @.30A
BOARD SIZE (mm)	86 X 89	102 X 102	130 X 150	106 X 102
AVE. ACCESS TIME (mS)	11.4	41.0	29.5	12.5
TEMPERATURE RANGE:				
OPERATIONAL (°C)	0 - 70	0 - 75	0 - 50	0 - 50
NON-VOLATILE (°C)	-40 - 100	-40 - 90	-40 - 80	-40 - 85
POWER DISSIPATION: (MAX)				
STANDBY (WATTS)	1.97	3.03	6.60	2.80
ACTIVE (WATTS)	3.91	6.70	10.7	4.80
ERROR CORRECTION	<3b BURST	<5b BURST	NONE	<3b BURST
MBM DEVICE WEIGHT (g)	28	74	34	28

TABLE 6.1

COMPARISON OF COMPETATIVE BUBBLE MEMORY SYSTEMS

cycle times. The Intel MBM system performs particularily poorly in these areas due to the low drive field frequency (i.e., the MBM propagation rate). The Intel burst data transfer rate, however, remains comparable to that of the other systems because the bubble device outputs two data bits per MBM cycle from two separate detector stacks.

The Motorola one megabit MBM system shows a distinct advantage in power supply requirements, physical board size, average access time and both standby and active power dissipations. The graph of Figure 6.1 clearly indicates the difference in power dissipation among the four bubble memory systems.

6.2 BUBBLES IN THE MEMORY HIERARCHY

As already discussed in earlier chapters, bubble memory devices are cyclic-access devices similar in architecture to that of floppy disks, hard disks, magnetic drums, and charge-coupled devices (CCDs). In comparison with these other cyclic-access storage media, bubble memories have faster access times, with the exception of CCDs (which have been limited to specialty markets since the introduction of the 64K DRAM). In total storage capacity, bubble memories rival that of the floppy disk and low capacity fixed-head disks as shown in Figure 6.2.

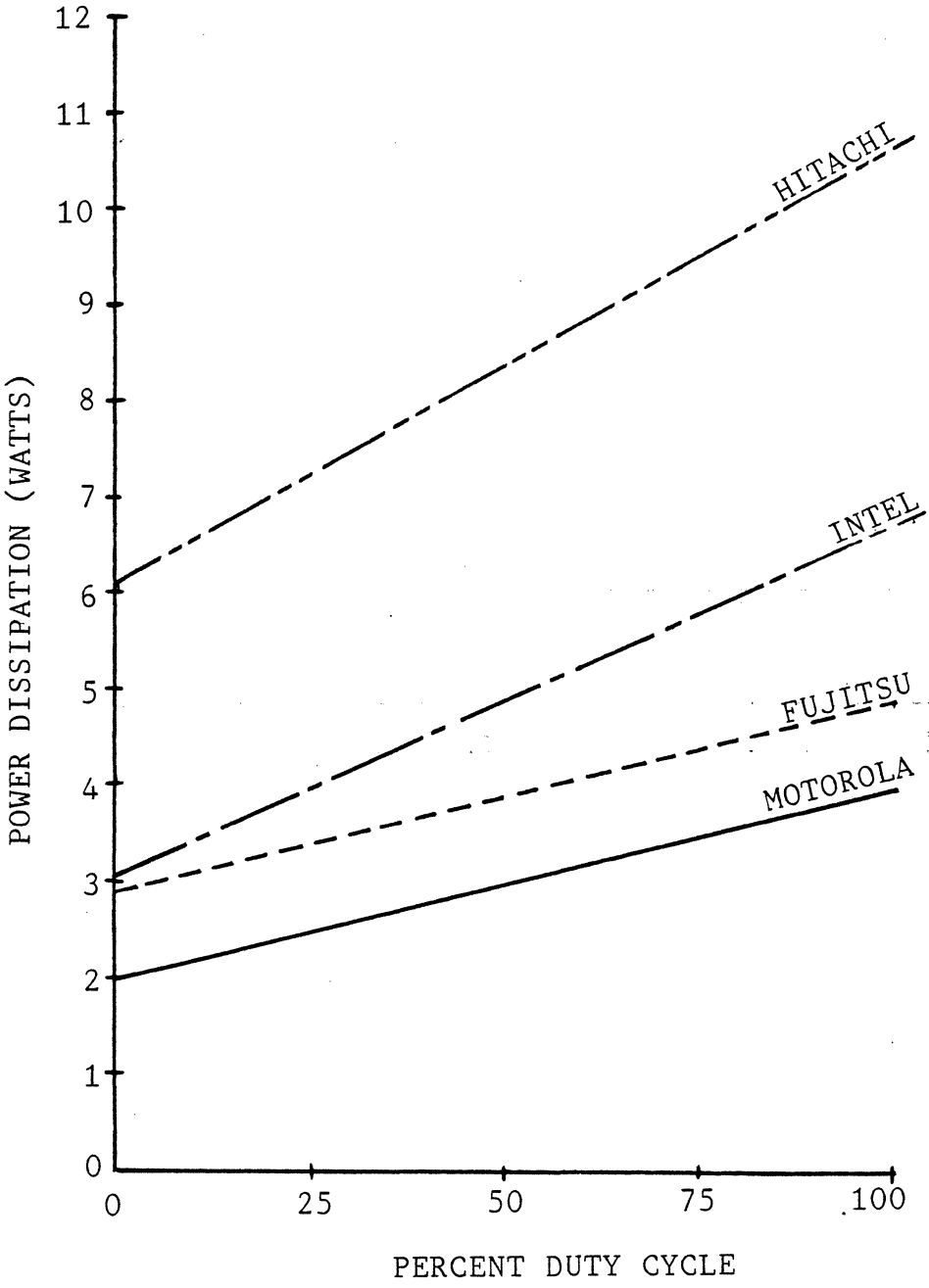
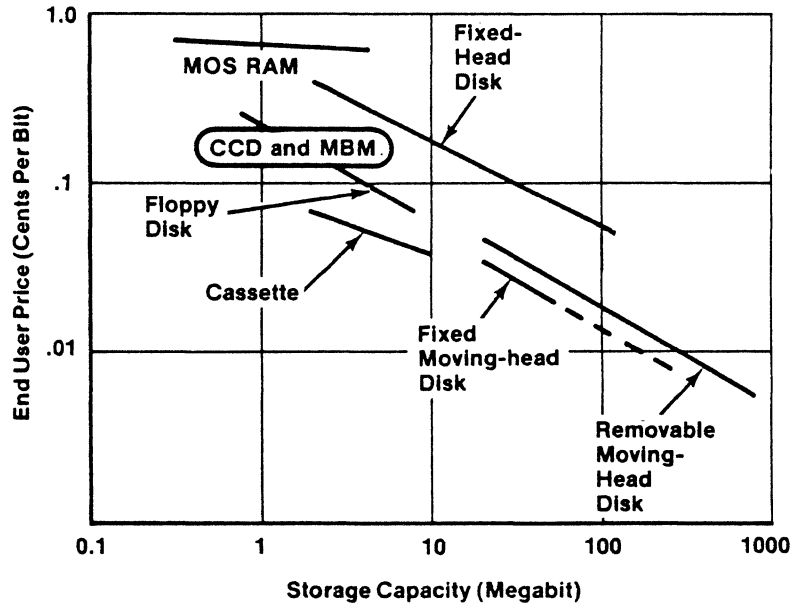


FIGURE 6.1

SYSTEM POWER DISSIPATION AS A FUNCTION OF DUTY CYCLE



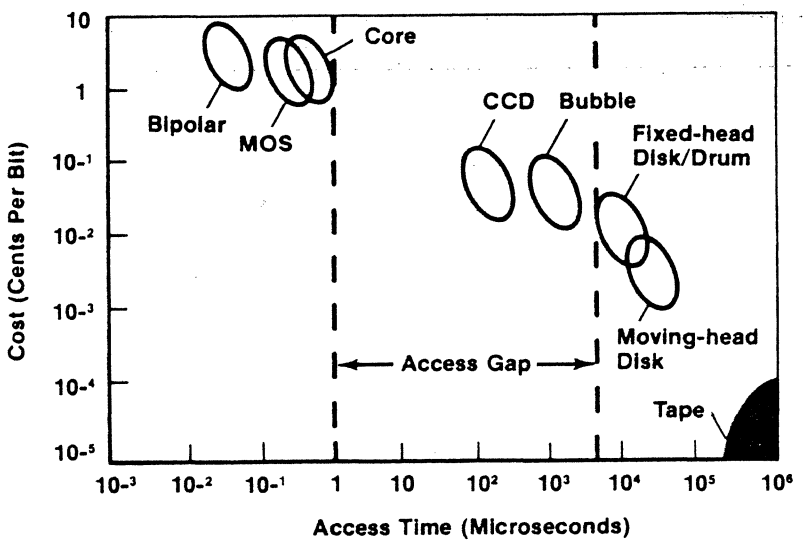


FIGURE 6.2

RELATIVE BUBBLE MEMORY STORAGE CAPACITY AND ACCESS TIME

The major advantages of bubble memories are that they are totally solid-state, are READ/WRITE memories, are non-volatile, are highly reliable, are small in size, lightweight, and insensitive to harsh environments and have a relatively fast access time. Table 6.2 tabulates the advantages of bubble memories over other storage devices.

This suggests that bubble memories have a place in the memory hierarchy in secondary storage and possibly even off-line data base storage as the memory capacity per package reaches the 4Mbit level and beyond. Initial costs may appear to be more expensive than floppy or hard disks, but when data loss, down time, and maintenance costs are added to the initial costs of floppies or hard disks, bubble memories appear to have yet another advantage. See Figure 6.3.

6.3 CONCLUSIONS

Bubble memories have been shown to be highly-reliable solid-state memory devices that have some distinct advantages over disk, drum and even semiconductor memory. They dissipate little power relative to disk and drum memory and also exhibit faster access times. For these reasons, bubble memories will most probably make inroads in the floppy disk and low-capacity hard disk markets. Rather than replace them entirely, though, bubble memory

ADVANTAGE	MEMORY DEVICE TYPE			
	DRAM	ROM, EPROM, EEPROM, SRAM	FLOPPY DISKS	HARD DISKS
NON-VOLATILE	X			
ALL SOLID-STATE			X	X
RELIABILITY			X	X
ADAPTABLE TO HARSH ENVIRONMENTS			X	X
VIBRATION INSENSITIVITY			X	X
EM NOISE IMMUNITY	X	X		
HIGH DENSITY PACKAGING	X	X		
WEIGHT			X	X
ACCESS TIME			X	X

TABLE 6.2

ADVANTAGES OF BUBBLES OVER OTHER MEMORY DEVICES

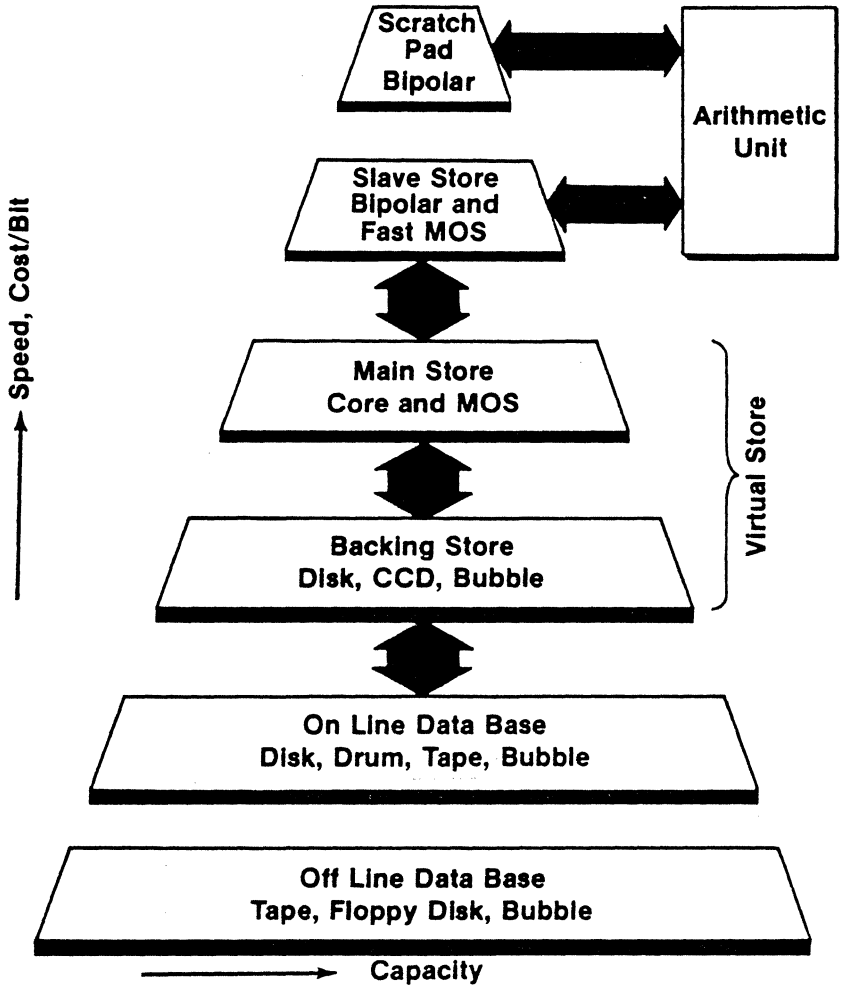

Scratch Pad Bipolar
Arithmetic Unit
Slave Store Bipolar and Fast MOS
Speed, Cost/Bit
Main Store Core and MOS
Virtual Store
Backing Store Disk, CCD, Bubble
On Line Data Base Disk, Drum, Tape, Bubble
Off Line Data Base Tape, Floppy Disk, Bubble
Capacity

FIGURE 6.3

BUBBLE MEMORIES IN THE MEMORY HIERARCHY

systems will more than likely complement disk and drum memory units and offer some new alternatives to these traditional storage media.

Furthermore, bubble memories will no doubt find applications in harsh environments like industrial control hardware. As pricing declines, the portable computer market may also prove to be a viable market for bubble memories, since they offer low power dissipation and non-volatile mass storage.

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APPENDIXES

APPENDIX A

BUBLTEST REFERENCE MANUAL

FEBRUARY 1984

B U B L T E S T

BUBBLE MEMORY SYSTEM TEST SOFTWARE PACKAGE REFERENCE MANUAL

MOTOROLA ENGINEERING RELEASE 1984

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REFERENCE MANUAL ORGANIZATION

The purpose of this reference manual is to provide a simple means of explaining how to use BUBLTEST (Rev 2.00) in the testing and evaluation of Motorola Bubble Memory Systems and their individual components. BUBLTEST has been designed to support Motorola's MBM2256 and MBM2011 family of bubble memory products.

Following a brief introduction to BUBLTEST, Chapter 2 deals with the minimum software and hardware system configuration required to support BUBLTEST (Rev 2.00).

Chapter 3 explains in detail the various features and options made available to the user via the menu-driven program structure.

Chapter 4 explains program loading, program set-up and system test execution of BUBLTEST from an EXORset development system.

Finally, Chapter 5 and Chapter 6 are the high-level flow-charts and source code listings, respectively.

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CHAPTER 1 -- INTRODUCTION

The BUBLTEST program is a diagnostic bubble memory system test program designed to exercise and test Motorola's 256K- and 1M-bit bubble memory devices, support circuits, and system-level products. It is delivered on a 5¼ inch mini-diskette and provides an easy means of exercising the bubble memory subsystem with its menu-driven structure. The program is designed to operate with Motorola's XDOS disk operating system software on EXORBUS-compatible hardware.

This document outlines the software structure of BUBLTEST and how it is intended to be used in testing Motorola's 256K- and 1M-bit bubble memory systems.

CHAPTER 2 — HARDWARE AND SOFTWARE REQUIREMENTS

The purpose of this chapter is to outline the hardware, firmware and software requirements for supporting the BUBLTEST (Rev 2.00) software package.

2.1 — Software Support Requirements

The minimum software and firmware required to support BUBLTEST (Rev 2.00) is as follows:

* XDOS disk operating system
* XORBUG monitor

2.2 — Hardware Support Requirements

The minimum hardware required to support BUBLTEST (Rev 2.00) is as follows:

* M6809 Microprocessor
* 32K RAM (minimum; memory address 0000-731F)
* CRT display
* ASCII Keyboard
* Floppy disk controller module
* 1 Floppy disk drive

* Bubble memory interface module with extension cable
* MBM2011EK Bubble memory evaluation kit

OR

* Bubble memory micromodule test board
* MBM Subsystem decode at C000-C007

Optional hardware supported by BUBLTEST includes:

* Model 781 Printer
* Model 703 Printer
* Printer interface module

Figure 2.1 shows the hardware organization of a typical bubble memory test system. An EXORset 30/30A/35 or 110 provides all that is required in hardware and software with the exception of the bubble memory hardware and optional printer. Therefore, it is strongly recommended that this software be operated on an EXORset development system.

Table 2.1 lists the memory address declarations for the bubble memory subsystem. These declarations must be strictly observed when designing in bubble memory hardware.

Figures 2.2 and 2.3 show the memory allocation for the BUBLTEST program in the EXORset 30/30A and EXORset 35/110 development systems, respectively.

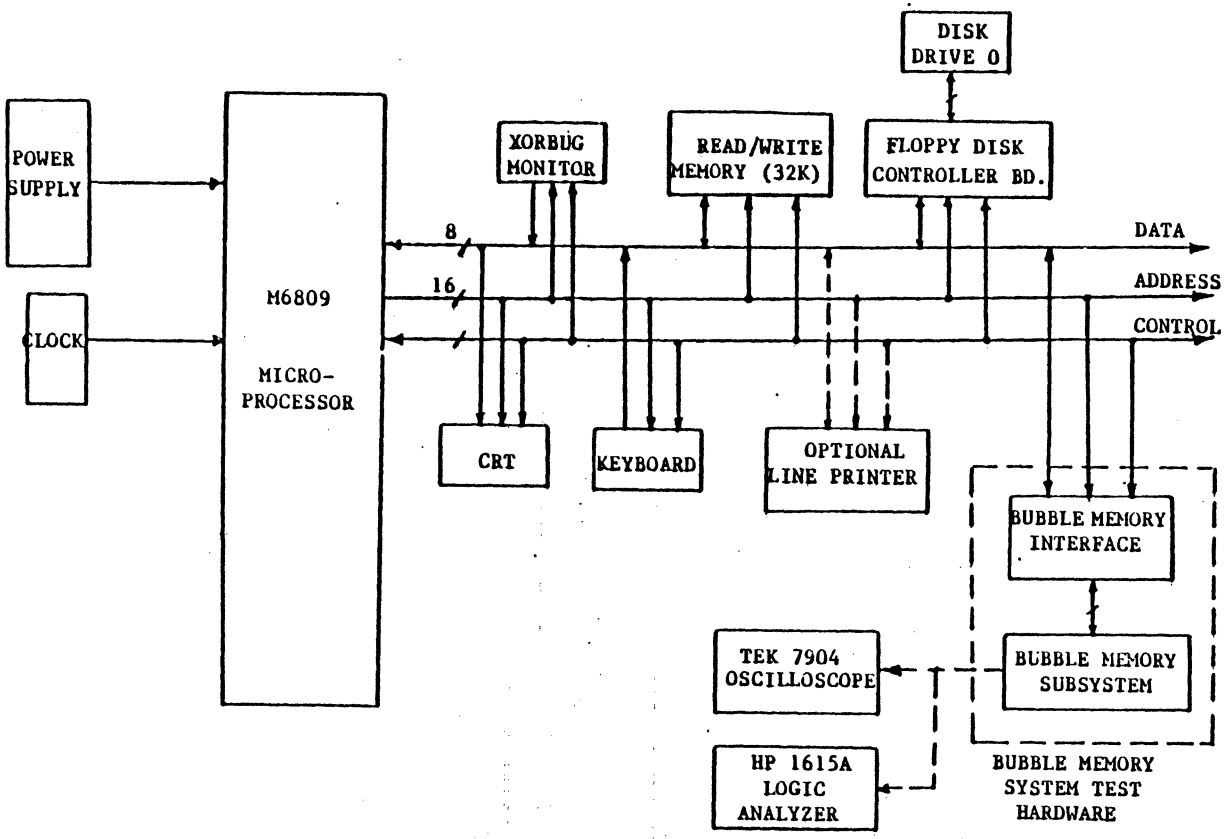


Figure 2.1 -- Typical Bubble Memory Test Hardware

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Table 2.1

BUBBLE MEMORY SUBSYSTEM ADDRESS DECLARATION

HEX ADDRESS	ACCESSED REGISTER
C000	COMMAND REGISTER
C001	MULTIPLE SECTOR REGISTER
C002	SECTOR ADDRESS REGISTER - LOW
C003	SECTOR ADDRESS REGISTER - HIGH
C004	RESIDUAL CONTROL REGISTER
C005	SYSTEM FEATURES REGISTER
C006	STATUS REGISTER
C007	FIFO BUFFER

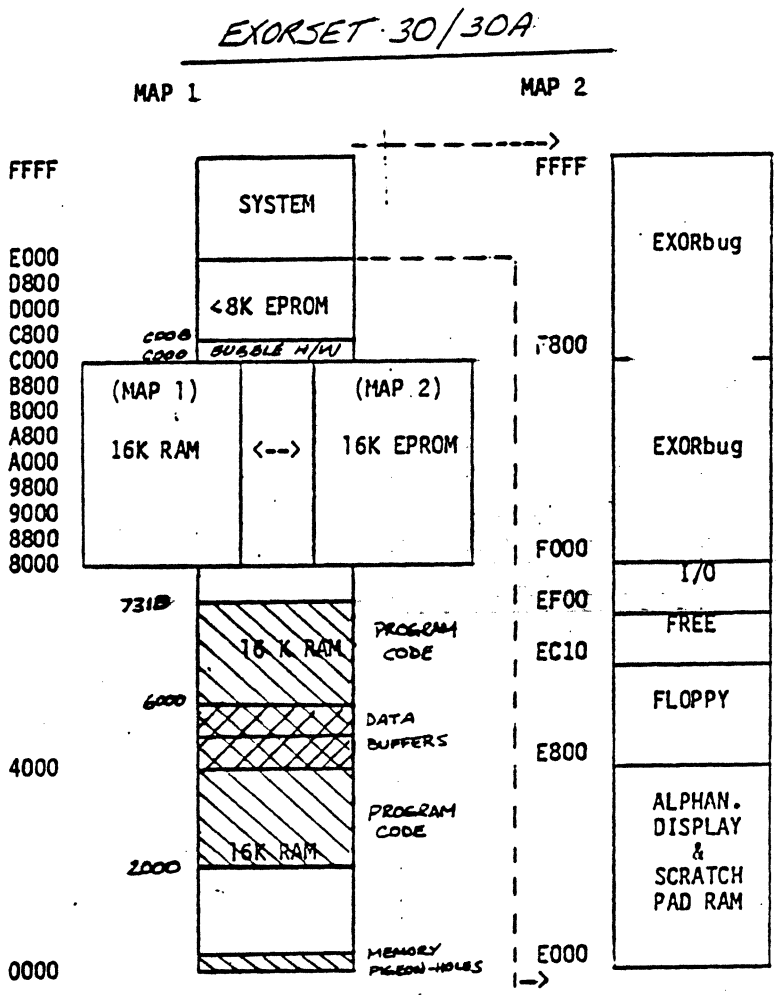


Figure 2.2 -- BUBLTEST Memory Allocation.

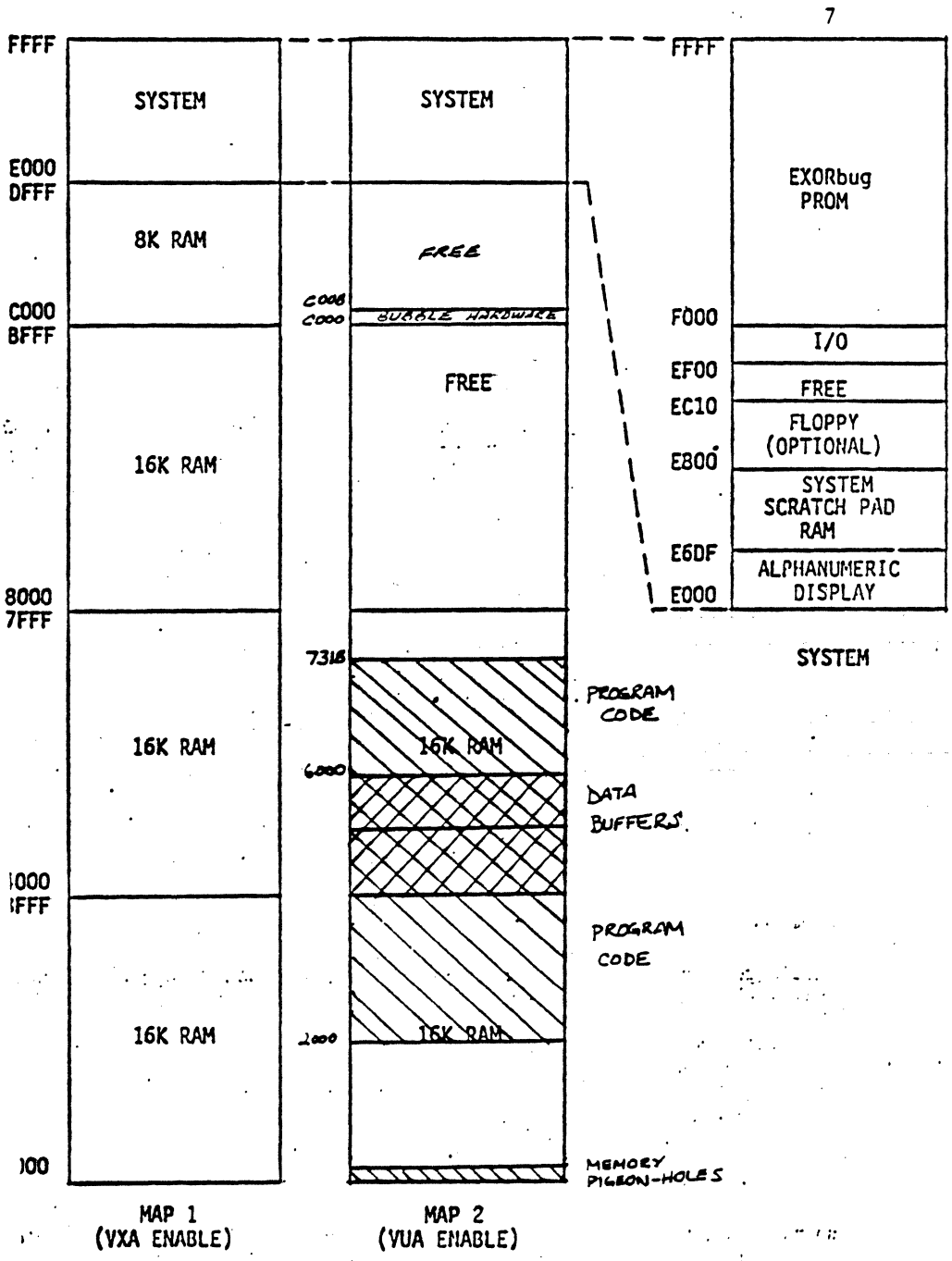


Figure 2.3 -- BUBLTEST Memory Allocation

8

2.3 -- Hardware Schematics

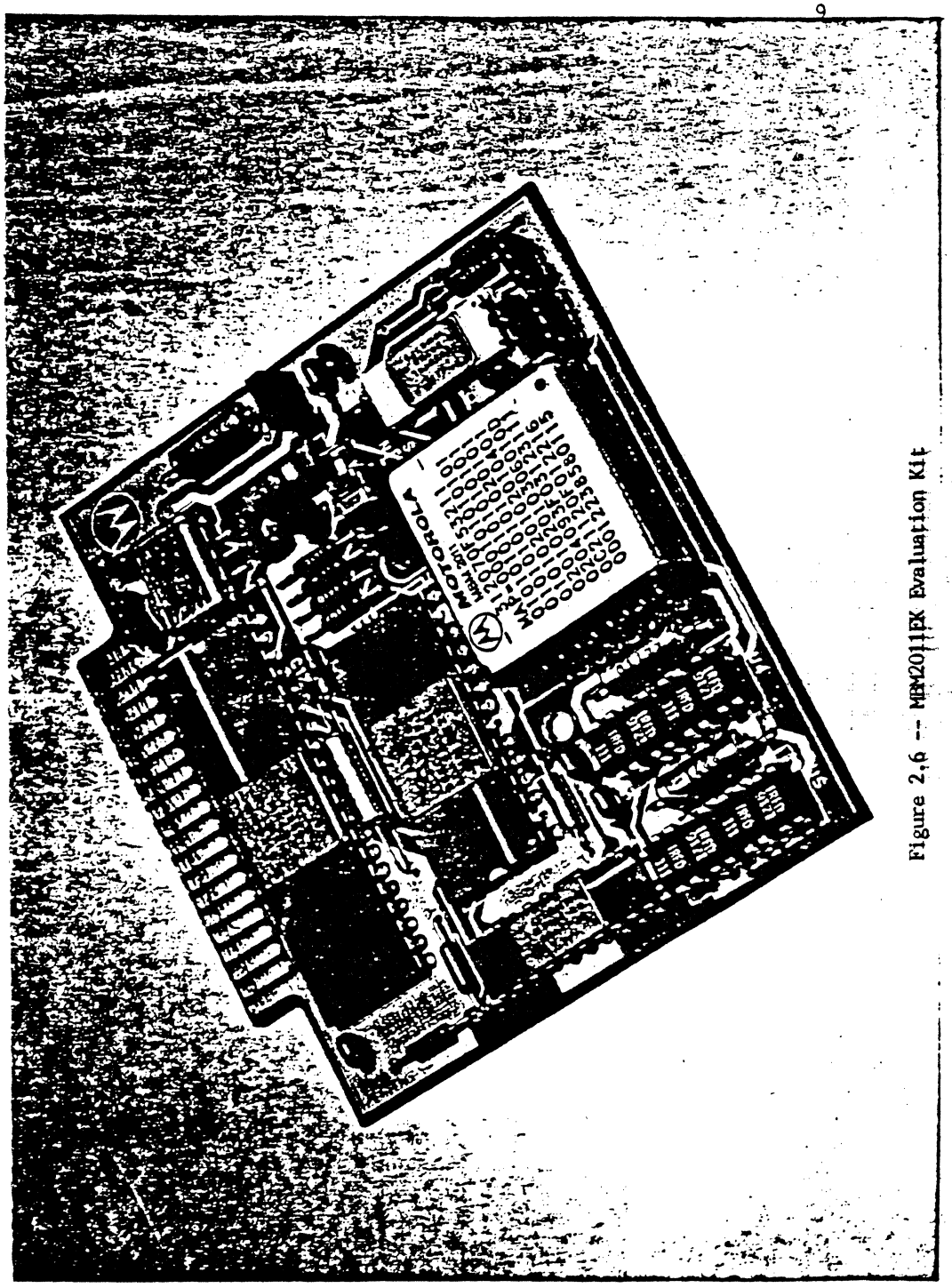


Figure 2,6 -- MEM2011EK Evaluation Kit

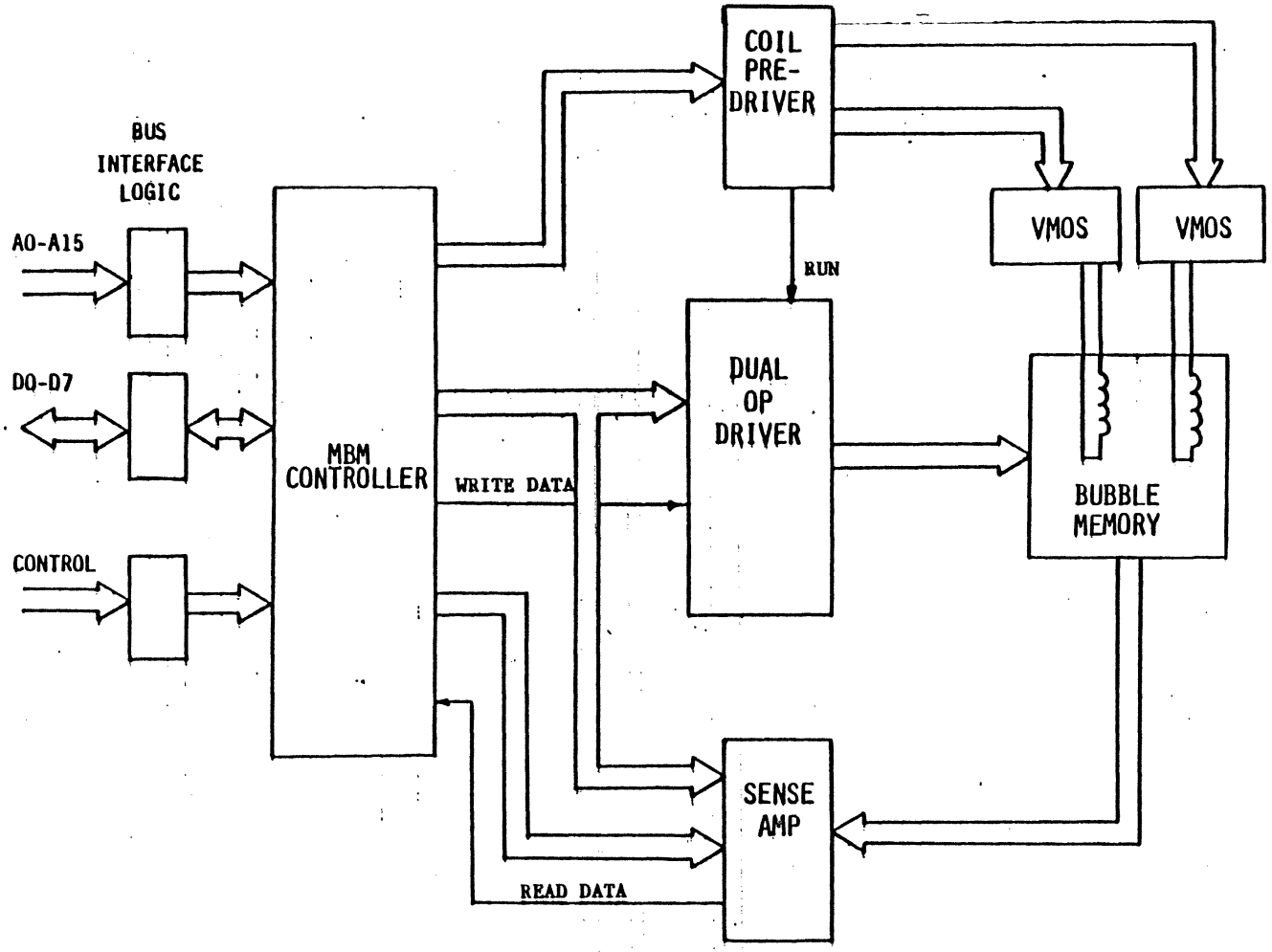


Figure 2.4

ONE-DEVICE BUBBLE MEMORY SYSTEM

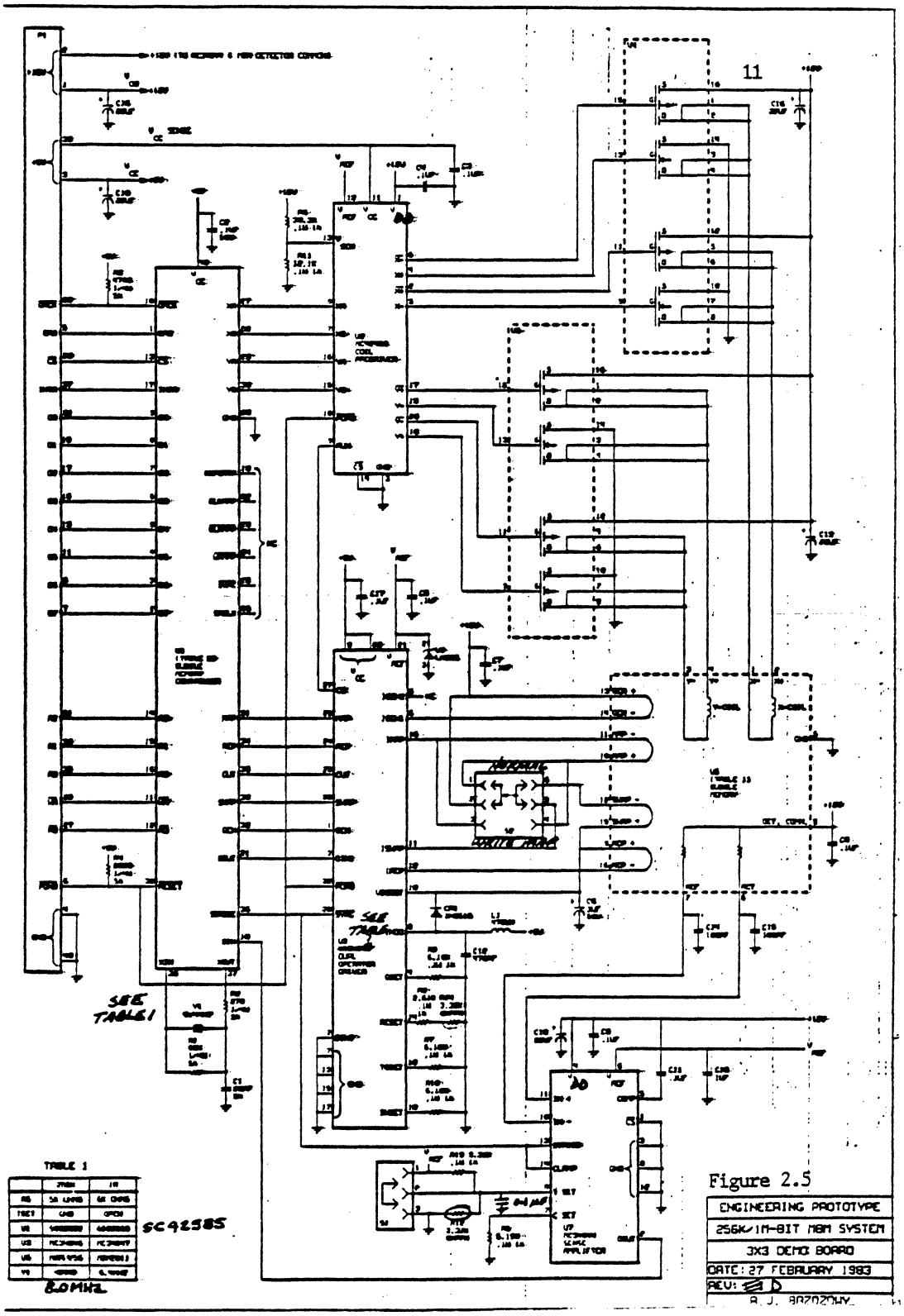

11
SEE TABLE 1
SEE TABLE
TABLE 1
SC42585
ENGINEERING PROTOTYPE
256K/1M-BIT MBM SYSTEM
3X3 DEMO BOARD
DATE: 27 FEBRUARY 1989
REV:
R. J. BAZOZOWY

Figure 2.5

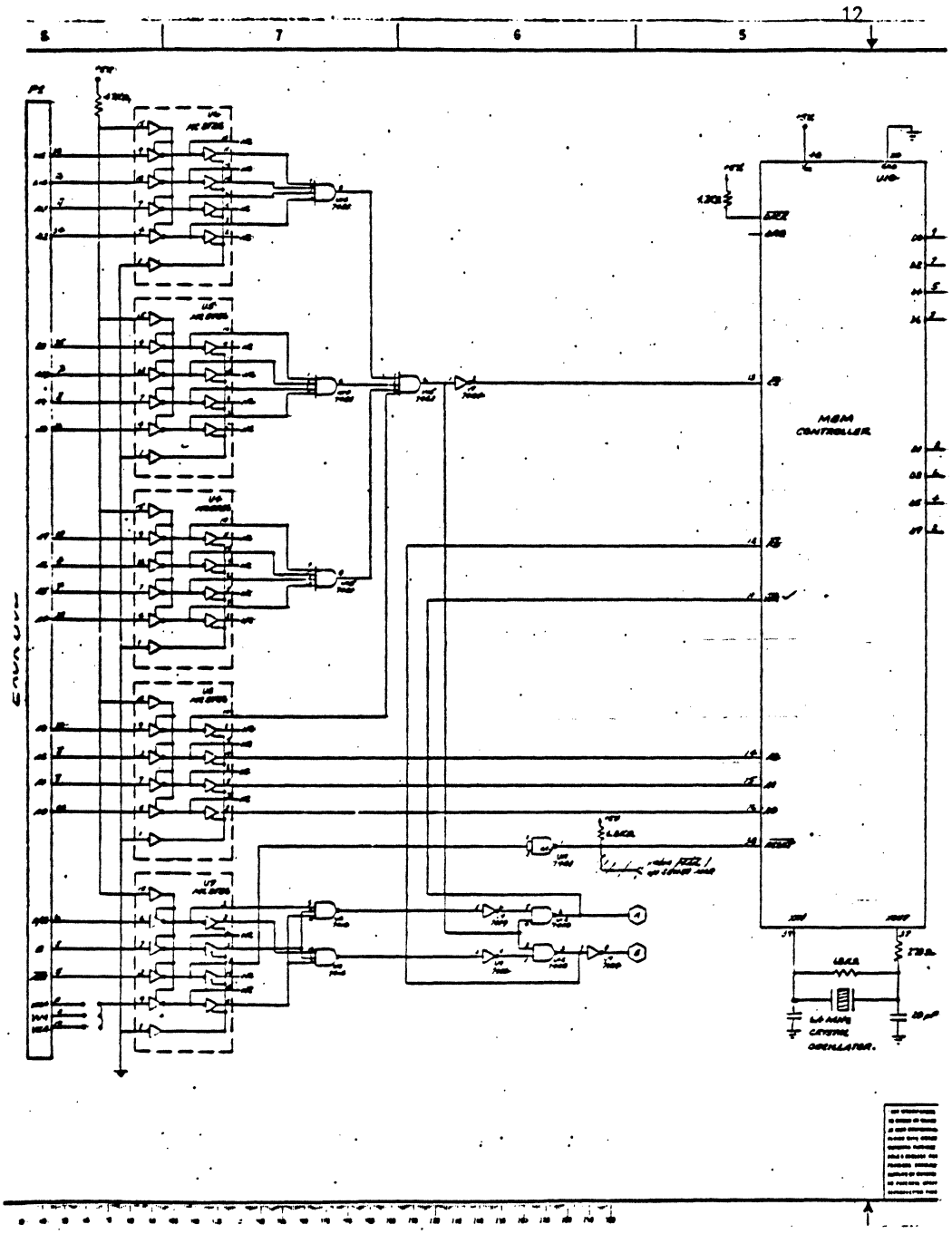


Figure 2.7 -- Bubble Memory Interface Logic

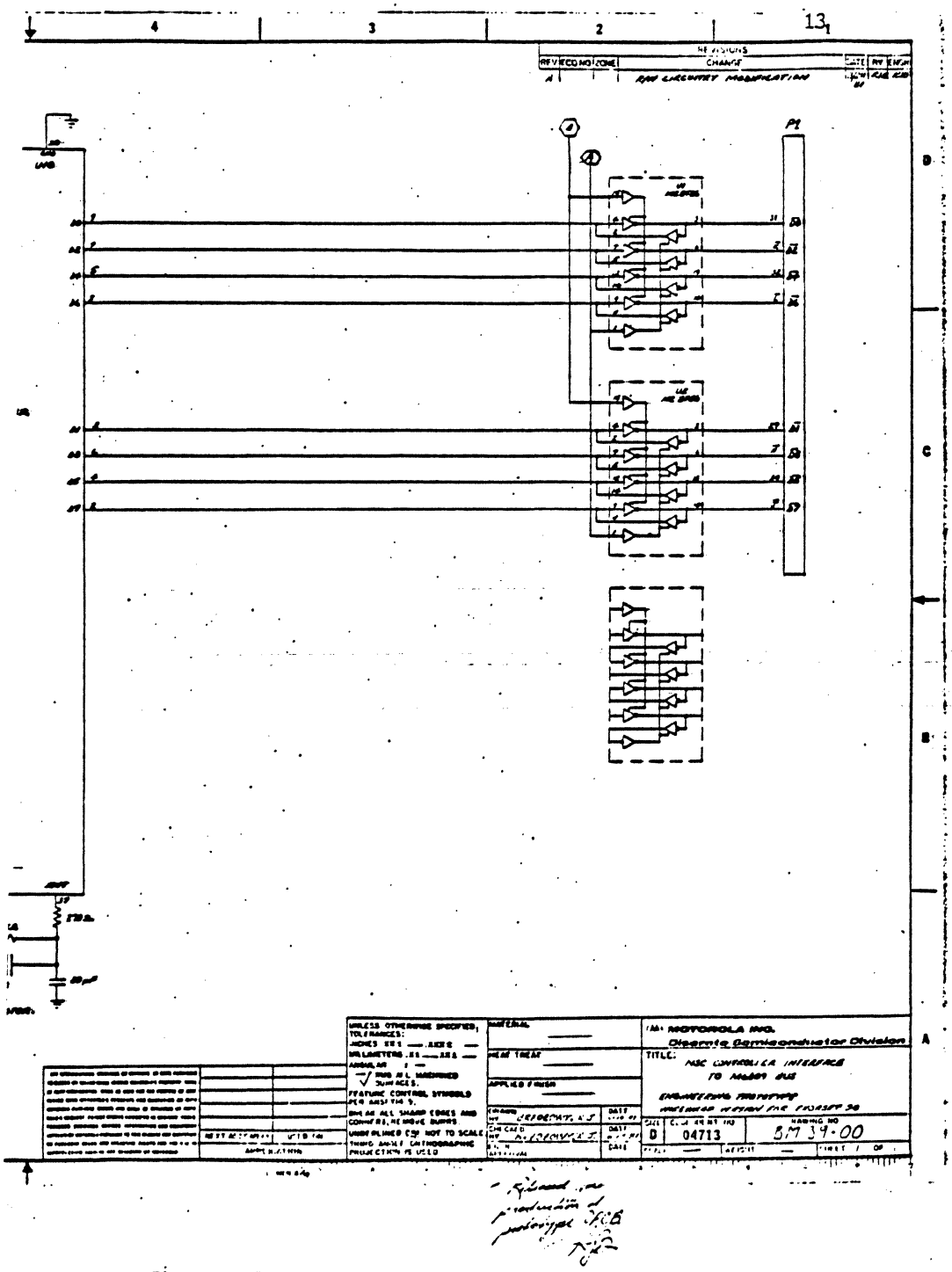


Figure 2.7a -- Bubble Memory Interface Logic

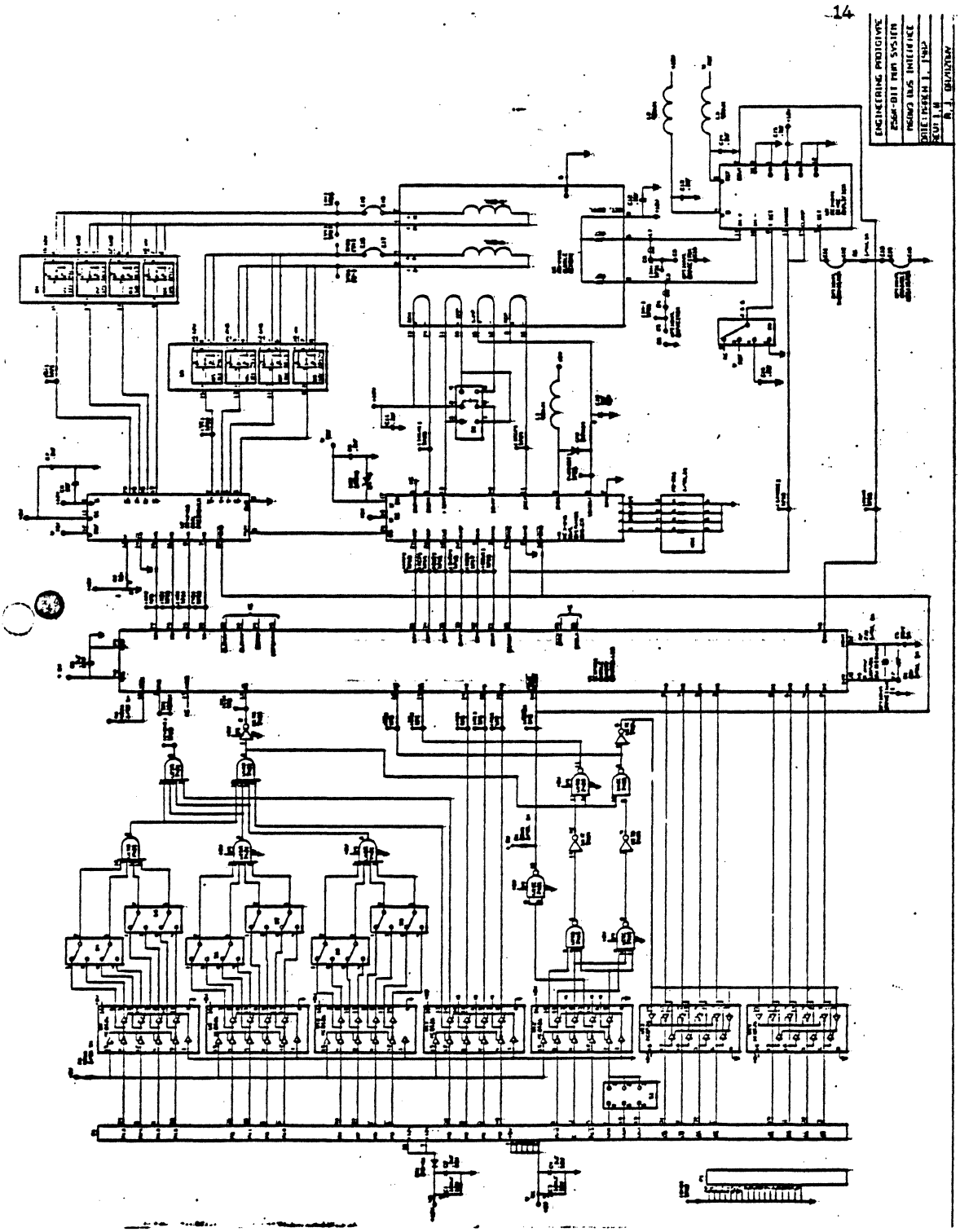


Figure 2.8 -- Bubble Memory Micromodule Test Board

CHAPTER 3 — BUBLTEST FEATURES AND OPTIONS

This chapter details the various features and options provided by BUBLTEST (Rev 2.00). It should be noted that BUBLTEST (Rev 2.00) will support only single-MBM operation. The software package MULTIBUB has been designed to accommodate single- and multiple-MBM operation.

3.1 — Main Program Menu

BUBLTEST (Rev 2.00) is a menu-driven software package that provides much flexibility in testing Motorola's 256K and 1M-bit bubble memory system products. Its menu organization makes it a useful tool for testing conducted by engineers, technicians and operators alike. Program execution, program set-up, and program alterations are accomplished by simply selecting options to jump from one level of the program to another. See Figure 3.1.

Once the program has been loaded from XDOS, the main program menu is displayed on the CRT terminal showing the various options available to the user. See Figure 3.2. Selection of any of the listed options by depressing the appropriate key executes the selected option or displays a subset of options available to the user. Once the options have been executed or changed, control can be returned to the main program menu.

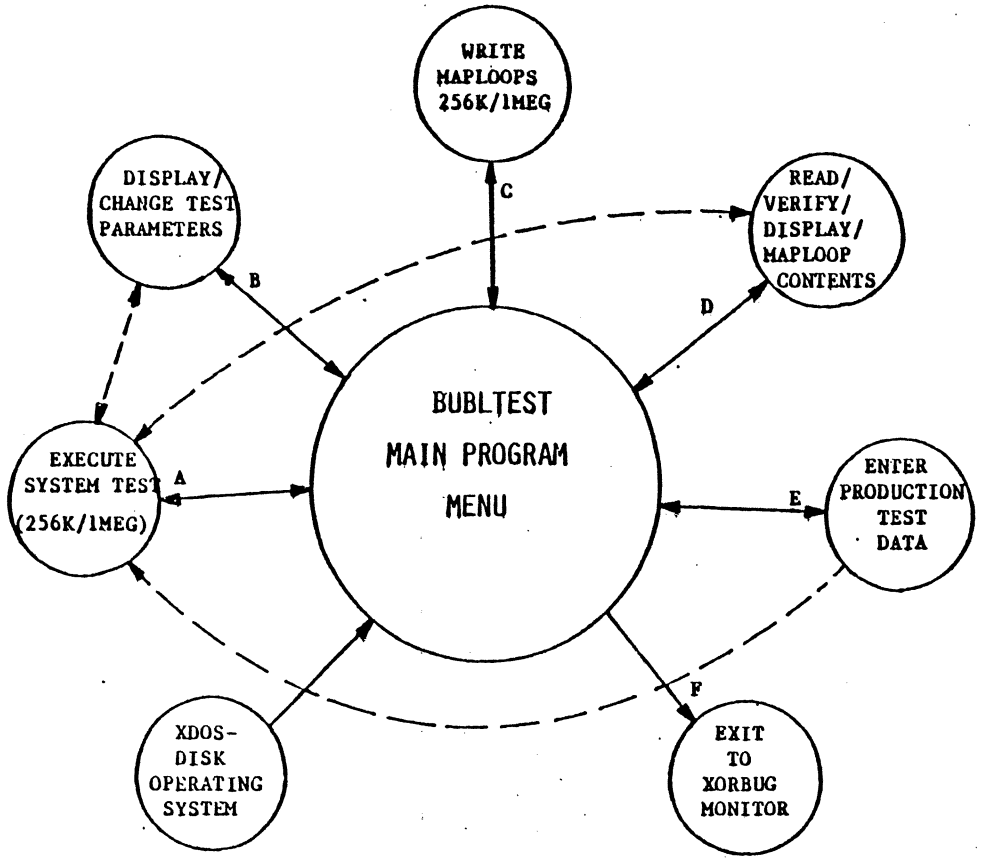


Figure 3.1 -- BUBLTEST Program Structure

17

```
**************************************************
*                                                *
*       BUBBLE MEMORY SYSTEM TEST                *
*             PROGRAM MENU                       *
*                                                *
**************************************************

  A. EXECUTE SYSTEM TEST
  B. DISPLAY/CHANGE TEST PARAMETERS
  C. EXECUTE MAPLOOP ALTER/WRITE
  D. READ AND DISPLAY MAPLOOP CONTENTS
  E. SET UP PRODUCTION TEST DATA
  F. EXIT TO XOREUG MONITOR
```

Figure 3.2 -- BUBLTEST Main Program Menu

3.2 -- Option A: Execute System Test

Selecting option A from the main program menu executes the system test function according to the test parameters listed in the current test status table (accessed via Option B). Upon selecting option A, the CRT display is clear and the program will indicate READY. A carriage return commences execution.

The system test consists of bubble memory system initializations, maploop reads and compares, full memory reads and writes, as well as documentation of any errors encountered throughout the test. Successful completion of the test sequence is acknowledged by a large PASS displayed on the screen (and line printer if selected) at the completion of the individual test. Any errors observed in the test will cause a FAIL to be displayed at the completion of the test.

Also displayed at the end of single-execution tests is a TRY AGAIN? (Y/N). A 'Y' entry from the keyboard will execute another system test, while an 'N' entry will transfer control back to the main program menu, once again displaying the option as depicted in Figure 3.2.

Figure 3.3 is a sample system test executed with a 1M-bit bubble memory subsystem.

```
 TRY AGAIN? (Y/N) Y
  ENTER DEVICE NUMBER: SAMPLE7                                  ** DEVICE #


DEVICE UNDER TEST: MOTOROLA 3X3 1 MEGABIT BOARDS
LOT # A0123456-8                                                ** TEST DATA
DATE: FEBRUARY 7,1984
TEMPERATURE: 25 DEGREES CELSIUS

BUBBLE MEMORY SYSTEM PRODUCTION TEST:
REVISION  2.00
MOTOROLA ENGINEERING RELEASE 1982                               ** START OF TEST

EXECUTING  50 INITIALIZATIONS
    SUCCESSFUL!!!!

EXECUTING MAP COMPARE TEST
    SUCCESSFUL!!!!

BUBBLE MEMORY DEVICE TYPE: MBM 2011  1M-BIT MEMORY
REDUNDANT LOOP NUMBERS:
 0000  0001  0002  0003  0004  0005  0006  0007  0008  0009
 0010  0013  0014  0016  0017  0018  0019  0020  0021  0022
 0024  0025  0026  0027  0029  0030  0031  0032  0033  0034
 0035  0043 *0051  0053  0054  0056  0063  0065  0074  0075
 0076  0085  0091  0101  0141  0192  0197 *0211  0212 *0232
*0283 *0292 *0370 *0374 *0375 *0376 *0392 *0569 *0580 *0581

* => NUMBER OF MASKED BAD LOOPS = 0013
     NUMBER OF MASKED WEAK LOOPS = 0047
TOTAL NUMBER OF REDUNDANT LOOPS = 0060                          ** MAPLOOP CONTENTS

EXECUTING WRITE/READ TEST
 TEST PASS NUMBER = 0009
DATA PATTERN= $00   # PAGES = 0128                              ** WRITE/READ TEST
DATA PATTERN= $08   # PAGES = 0128
DATA PATTERN= $18   # PAGES = 0128
DATA PATTERN= $38   # PAGES = 0128
DATA PATTERN= $78   # PAGES = 0128
DATA PATTERN= $F8   # PAGES = 0128
DATA PATTERN= $F9   # PAGES = 0128
DATA PATTERN= $FB   # PAGES = 0128
DATA PATTERN= $FF   # PAGES = 0128
PSEUDO-RANDOM DATA # PAGES = 0896


**********************
PPP   AA   SS   SS
P  P A  A S  S S  S
P  P A  A S    S
PPP  AAAA  SS   SS                                              ** SUCCESSFUL
P    A  A    S    S                                             COMPLETION
P    A  A S  S S  S                                             OF TEST
P    A  A  SS   SS
**********************
```

Figure 3.3 -- Sample System Test Printout

3.3 -- Option B: Display/Change Test Parameters

Selecting option B from the main program menu causes the CURRENT TEST STATUS table of Figure 3.4 to be displayed. The upper half of the table lists the current constant data patterns and the corresponding number of pages to be written with that data. The remaining unused pages are filled with pseudo-random data generated by the algorithm listed in Chapter 7 of this document. A maximum of nine constant data patterns are allowed. The maximum number of pages is 225 ($FF), while the minimum is one ($01). Random data patterns are started when a table entry of DATA PATTERN = $00 # PAGES = $00 in an entry other than the first entry is encountered or the maximum of nine data patterns is reached.

The lower half of the CURRENT TEST STATUS table lists options available for system test execution. The number of full memory reads per full memory write can be set from one to 256 ($01 to $00).

Turning the line printer on allows for documentation of test results via a line printer interfaced to the bubble memory system test unit. In long-term tests, however, this option should be left in the OFF state with the line printer selected. In this mode, only errors encountered in the WRITE/READ test are documented via the printer.

```
C U R R E N T    T E S T    S T A T U S
-----------------------------------------

DATA PATTERN= $00   # PAGES = $10
DATA PATTERN= $01   # PAGES = $10
DATA PATTERN= $03   # PAGES = $10
DATA PATTERN= $07   # PAGES = $10
DATA PATTERN= $0F   # PAGES = $10
DATA PATTERN= $1F   # PAGES = $10
DATA PATTERN= $3F   # PAGES = $10
DATA PATTERN= $7F   # PAGES = $10
DATA PATTERN= $FF   # PAGES = $10
PSEUDO-RANDOM DATA # PAGES = (REMAINING PAGES)


#FULL MEMORY READS/WRITE:   02
LINE PRINTER STATUS:        [ ON]
READ-ONLY MODE STATUS:      [OFF]
AUTO-PATTERN CHANGE MODE:   [ ON]
CONTINUOUS EXECUTION:       [OFF]
        HALT ON ERROR:      [ ON]


      CHANGE? (Y or N)
```

Figure 3.4 -- Current Test Status Table

The READ-ONLY option (when set to ON) allows for skipping over the full-memory write protion of the test, thereby reading the full memory and comparing the read data with the expected data listed in the upper half of the CURRENT TEST STATUS table. Care must be exercised to ensure that the upper half of the CURRENT TEST STATUS table corresponds exactly to that written previously in the bubble memory.

This option is frequently used in tests conducted for non-volatile storage. For this test a specific set of patterns are entered into the upper half of the table with the AUTO-CHANGE PATTERN option OFF. The system test is executed with READ-ONLY MODE: OFF. Upon successful completion of the system test, the bubble memory is subjected to a non-volatile storage test (e.g., extreme temperature). Upon completion and stabilization of the MMM, the bubble memory is then again system tested with the READ-ONLY MODE: ON.

The AUTO PATTERN CHANGE option provides for automatically changing data patterns and random data following the completion of every test sequence. This is particularly useful in long-term tests to ensure that new data is written to/read from the storage loops every execution of the test.

The CONTINUOUS EXECUTION option provides for long-term unattended testing of bubble memory subsystems. Used in conjunction with a line printer (LINE PRINTER STATUS: OFF), the AUTO CHANGE PATTERN: ON and

HALT ON ERROR: OFF, error rate and longevity testing can be conducted. Any errors will cause the printer to record the event, but system execution will continue. Also, every 10,000 completions of the test will cause a "10,000 passes complete" to be printed.

If a line printer is not available, the HALT ON ERROR can be set to ON, thereby halting execution at the end of the current test sequence until the error information can be manually documented. The user can then continue execution or return control to the main program menu.

CHANGING OPTIONS:

Entering a 'Y' in response to 'CHANGE? (Y/N)' causes the cursor to move to the top of the data pattern table. The program will now accept entries of valid hexadecimal characters for data patterns and number of pages. A carriage return always moves the cursor to the next entry. A line feed will move the cursor from the upper table to the first entry in the lower table. (In the lower table, the line feed and carriage return react identically.) Note that the DATA PATTERN = $00 # PAGES = $00 causes the random data generation to begin.

In the lower table, the options can be toggled from ON to OFF or OFF to ON by entering an '@' when the cursor is aligned. After entering all options, return the cursor to the CHANGE? (Y/N) message

by entering carriage returns or line feeds. Entering a 'N' in response to CHANGE? (Y/N) will return control to the main program menu.

3.4 -- Option C: Change/Write Maploop Contents

Selecting the C option from the main program menu clears the CRT screen and causes the CHANGE/WRITE MAPLOOP CONTENTS menu to be displayed. Two options are currently available (also an option to return control to the main program menu). See Figure 3.5.

OPTION A: ALTER EXISTING MAP DATA

If the maploop contents are to be appended with bad loops not currently masked, the A option: ALTER EXISTING MAPLOOP DATA is selected. This causes the current contents of the maploop to be read and displayed. (If an error is encountered through, execution is suspended and option B: WRITE NEW MAP DATA must be used.)

The program then requests the decimal value corresponding to the bad loop number to be entered. Provided the loop is not already masked and a weak loop exists which can be masked good, the map contents stored in a buffer will be adjusted to accommodate the appended loop.

If more loops are to be appended, enter 'N' in response to 'WRITE MAP? (Y/N)' and 'Y' in response to 'ANOTHER LOOP? (Y/N).

```
**************************************************
*                                                *
*          BUBBLE  MEMORY  BOOTLOOP              *
*           ALTER / WRITE  PROGRAM               *
*                                                *
**************************************************

     A.  ALTER EXISTING MAPLOOP DATA
     B.  WRITE NEW MAPLOOP DATA
     C.  RETURN TO PROGRAM MENU
```

Figure 3.5 -- Write Maploop Menu

The program again requests decimal loop number input. This can be repeated until all loops are appended, at which time a 'Y' should be entered in response to 'WRITE MAP? (Y/N)'.

At this time, the bubble memory should be cleared and the mechanical interlock changed for map write operations. Entering the appropriate maploop number causes the map to be written with the new maploop data.

The mechanical interlock must now be returned to the normal position. A carriage return causes the main program menu to be displayed. See Figure 3.6.

OPTION B: WRITE NEW MAPLOOP DATA

When maploop data is entered from the bubble memory label, option B of the CHANGE/WRITE MAPLOOP CONTENTS menu is used.

A buffer is formatted with the proper synchronization pattern in response to the device type (i.e., MEGABIT versus 256K). The CRT screen is first cleared, then a bubble memory label is displayed. See Figure 3.7. Data is now entered exactly as on the device label. Carriage returns are automatically inserted, so that the user simply enters the coded information character-by-character.

When all information is entered, the proposed maploop contents are displayed. The bubble memory must now be cleared and the

```
C

          ********************************************
          *                                          *
          *        BUBBLE  MEMORY  BOOTLOOP          *
          *          ALTER / WRITE  PROGRAM          *
          *                                          *
          ********************************************

               A.  ALTER EXISTING MAPLOOP DATA
               B.  WRITE NEW MAPLOOP DATA
               C.  RETURN TO PROGRAM MENU

          SELECT OPTION: A
EXECUTING  50 INITIALIZATIONS
    SUCCESSFUL!!!!

EXECUTING MAP COMPARE TEST
    SUCCESSFUL!!!!

BUBBLE MEMORY DEVICE TYPE: MBM 2011  1M-BIT MEMORY
REDUNDANT LOOP NUMBERS:
 0000  0001  0002  0003  0004  0005  0006  0007  0008  0009
 0010  0013  0014  0016  0017  0018  0019  0020  0021  0022
 0024  0025  0026  0027  0029  0030  0031  0032  0033  0034
 0035  0043 *0051  0053  0054  0056  0063  0065  0074  0075
 0076  0085  0091  0101  0141  0192  0197 *0211  0212 *0232
*0283 *0292 *0370 *0374 *0375 *0376 *0392 *0569 *0580 *0581

* => NUMBER OF MASKED BAD LOOPS = 0013
     NUMBER OF MASKED WEAK LOOPS = 0047
TOTAL NUMBER OF REDUNDANT LOOPS = 0060

 ENTER 3-DIGIT LOOP NUMBER TO BE MASKED AS BAD: 210

REDUNDANT LOOP NUMBERS:
 0001  0002  0003  0004  0005  0006  0007  0008  0009  0010
 0013  0014  0016  0017  0018  0019  0020  0021  0022  0024
 0025  0026  0027  0029  0030  0031  0032  0033  0034  0035
 0043 *0051  0053  0054  0056  0063  0065  0074  0075  0076
 0085  0091  0101  0141  0192  0197 *0210 *0211  0212 *0232
*0283 *0292 *0370 *0374 *0375 *0376 *0392 *0569 *0580 *0581

* => NUMBER OF MASKED BAD LOOPS = 0014
     NUMBER OF MASKED WEAK LOOPS = 0046
TOTAL NUMBER OF REDUNDANT LOOPS = 0060

   EXECUTE MAP WRITE ? (Y/N) N       ANOTHER LOOP ? (Y/N) Y
 ENTER 3-DIGIT LOOP NUMBER TO BE MASKED AS BAD: 099

REDUNDANT LOOP NUMBERS:
 0002  0003  0004  0005  0006  0007  0008  0009  0010  0013
 0014  0016  0017  0018  0019  0020  0021  0022  0024  0025
 0026  0027  0029  0030  0031  0032  0033  0034  0035  0043
*0051  0053  0054  0056  0063  0065  0074  0075  0076  0085
 0091  0101  0141  0192  0197 *0209 *0210 *0211  0212 *0232
*0283 *0292 *0370 *0374 *0375 *0376 *0392 *0569 *0580 *0581

* => NUMBER OF MASKED BAD LOOPS = 0015
     NUMBER OF MASKED WEAK LOOPS = 0045
TOTAL NUMBER OF REDUNDANT LOOPS = 0060


   EXECUTE MAP WRITE ? (Y/N) Y
READY TO EXECUTE MAP WRITE
CHANGE THE CONFIGURATION JUMPERS FOR WRITE
TRANSFER COMPLETE.    STATUS = 01

RETURN JUMPERS TO ORIGINAL POSITION
  OR TO CONTINUE
```

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* OPTION C SELECTED FROM MAIN MENU.

* OPTION A - CHANGE EXISTING MAPLOOP INFO.

* PROGRAM READS, VERIFIES, AND DISPLAYS CURRENT MAPLOOP INFO.

* BAD LOOP NUMBER TO BE APPENDED IS ENTERED. (DECIMAL VALUE)

* UPDATED MAPLOOP CONTENTS DISPLAYE

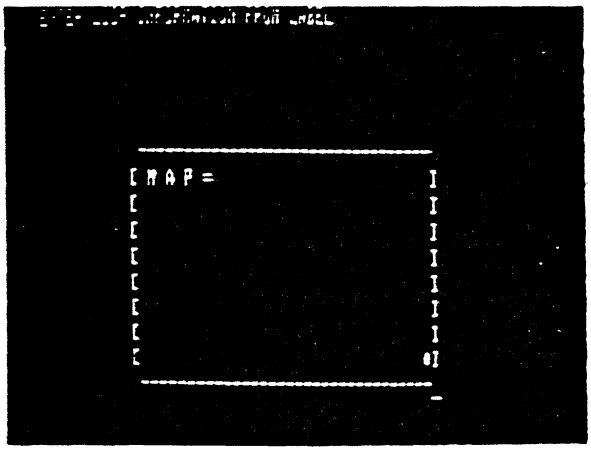
* PROGRAM REQUESTS WHETHER MAP IS TO BE WRITTEN OR ADDITIONAL LOOPS ARE TO BE APPENDED.

* READY FOR MAP WRITE - DEVICE MUST BE CLEARED AT THIS TIME.

* STATUS DISPLAYED.

Figure 3.6 -- Sample Maploop Alteration

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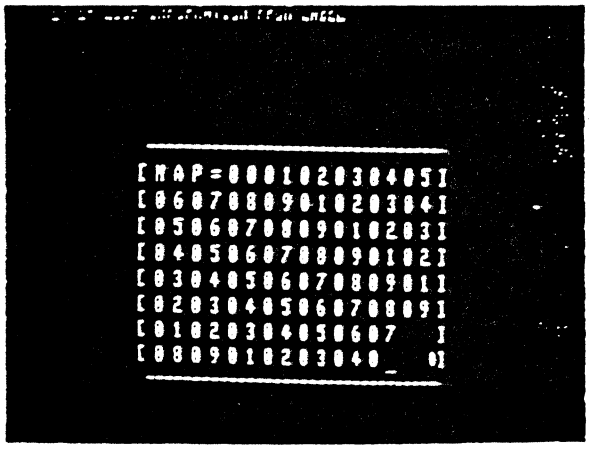


Figure 3.7 -- Write New Maploop Display

mechanical interlock set for the write map operation. Entering the appropriate maploop number causes the map to be written with the entered maploop data.

The mechanical interlock must now be returned to the normal position. A carriage return causes the main program menu to be displayed.

3.5 — Option D: Display/Verify Maploop Contents

Selecting option D: DISPLAY/VERIFY MAPLOOP CONTENTS from the main program menu executes only the system initialization, map read and map display sequences of the system test. This option is used primarily to read maploop contents only. A 'TRY AGAIN? (Y/N)' message at the end of each map read and display allows for repetitive map read operations. A 'N' in response to 'TRY AGAIN? (Y/N) returns control the main program menu. See Figure 3.8.

3.6 -- Option E: Enter Test Data

Selecting option E: ENTER TEST DATA from the main program allows test conditions to be entered in a buffer memory accessible by the system test. Such data includes the DATE, DEVICE UNDER TEST, LOT #, and TEMPERATURE and is useful in production testing. A carriage return allows termination of entered data and access to

30

```
Y
EXECUTING  50 INITIALIZATIONS
    SUCCESSFUL!!!!

EXECUTING MAP COMPARE TEST
    SUCCESSFUL!!!!

BUBBLE MEMORY DEVICE TYPE: MBM 2011  1M-BIT MEMORY
REDUNDANT LOOP NUMBERS:
 0000  0001  0002  0003  0004  0005  0006  0007  0008  0009
 0010  0013  0014  0016  0017  0018  0019  0020  0021  0022
 0024  0025  0026  0027  0029  0030  0031  0032  0033  0034
 0035  0043 *0051  0053  0054  0056  0063  0065  0074  0075
 0076  0085  0091  0101  0141  0192  0197 *0211  0212 *0232
*0283 *0292 *0370 *0374 *0375 *0376 *0392 *0569 *0580 *0581

* => NUMBER OF MASKED BAD LOOPS = 0013
    NUMBER OF MASKED WEAK LOOPS = 0047
TOTAL NUMBER OF REDUNDANT LOOPS = 0060


 TRY AGAIN? (Y/N)
```

Figure 3.8 -- Sample DISPLAY/VERIFY MAPLOOP CONTENTS

the next data category. If only a carriage return is entered, the data remains as is. Figure 3.9 is an example of data entered under the E option. Following data entry of the last category, control is returned to the main program menu.

During the execution of the system test (option A), this data is retrieved from the buffer memory and documented onto every test sheet as shown in Figure 3.10.

As test conditions change, the buffer memory can be updated by again exercising option E and entering a carriage return where data is to remain as is.

3.7 -- Option F: Return to XORBUG

Selecting option F from the main program menu allows control to be transferred to the XORBUG monitor resident in the system firmware. Re-entry into BUBLTEST must then be accomplished through XDOS.

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E

DATE: FEBRUARY 8, 1984
DEVICE UNDER TEST: MBM2011A - 14mU
LOT # A0654321-8
TEMPERATURE: 65 DEGREES CELSIUS

Figure 3.9 -- Sample Test Data Entry

```
 ENTER DEVICE NUMBER: SAMPLE4                                  **DEVICE NUMBER

                                                                      33
DEVICE UNDER TEST: MOTOROLA 3X3 1 MEGABIT BOARDS
LOT # A0123456-8                                               **TEST DATA
DATE: FEBRUARY 7,1984
TEMPERATURE: 25 DEGREES CELSIUS

BUBBLE MEMORY SYSTEM PRODUCTION TEST:
REVISION  2.00
MOTOROLA ENGINEERING RELEASE 1982                              **START OF TEST

EXECUTING  50 INITIALIZATIONS
    SUCCESSFUL!!!!                                             ** SYSTEM INITIALIZA-
                                                                  TION
EXECUTING MAP COMPARE TEST
    SUCCESSFUL!!!!

BUBBLE MEMORY DEVICE TYPE: MBM 2011  1M-BIT MEMORY
REDUNDANT LOOP NUMBERS:
 0000  0001  0002  0003  0004  0005  0006  0007  0008  0009
 0010  0013  0014  0016  0017  0018  0019  0020  0021  0022
 0024  0025  0026  0027  0029  0030  0031  0032  0033  0034
 0035  0043 *0051  0053  0054  0056  0063  0065  0074  0075
 0076  0085  0091  0101  0141  0192  0197 *0211  0212 *0232
*0283 *0292 *0370 *0374 *0375 *0376 *0392 *0569 *0580 *0581

* => NUMBER OF MASKED BAD LOOPS = 0013
     NUMBER OF MASKED WEAK LOOPS = 0047
TOTAL NUMBER OF REDUNDANT LOOPS = 0060                         ** MASKED LOOP SET

EXECUTING WRITE/READ TEST
 TEST PASS NUMBER = 0006                                       **WRITE/READ TEST
DATA PATTERN= $00  # PAGES = 0128
DATA PATTERN= $04  # PAGES = 0128
DATA PATTERN= $0C  # PAGES = 0128
DATA PATTERN= $1C  # PAGES = 0128
DATA PATTERN= $3C  # PAGES = 0128
DATA PATTERN= $7C  # PAGES = 0128
DATA PATTERN= $FC  # PAGES = 0128
DATA PATTERN= $FD  # PAGES = 0128
DATA PATTERN= $FF  # PAGES = 0128
PSEUDO-RANDOM DATA # PAGES = 0896


**********************                                         **SUCCESSFUL COMPLETIC
PPP    AA    SS    SS                                           OF TEST
P  P  A  A  S   S S   S
P  P A   A S     S
PPP  AAAA  SS    SS
P    A  A     S     S
P    A  A S   S S   S
P    A  A  SS    SS
**********************
```

Figure 3.10 -- Sample Test Sheet Depicting Test Data

CHAPTER 4 -- USING BUBLTEST

This chapter describes how to load, set-up and execute BUBLTEST test sequences.

4.1 -- Program Loading

BUBLTEST (Rev 2.00) is loaded into system memory using XDOS. First XDOS must be initialized using the 'XDOS' command in response to the XDRBUG prompt. Once the '=' appears, simply enter 'BUBLTEST' followed by a carriage return. The program will automatically load itself into system memory and begin program execution by displaying the main program menu. BUBLTEST is now ready for use.

4.2 -- Program Set-up

Test parameters can now be entered (if desired) via option B (See Section 3.3) and test data recorded (if desired) via option E (See Section 3.6).

Test execution or exercising any option is possible at this time.

4.3 -- Test Execution

With all test parameters entered and all test data recorded, test execution can begin by selecting option A. The system will respond with READY. A carriage return results in a request for the device number. An entry followed by another carriage return begins program execution.

CHAPTER 5
BUBLTEST EXECUTION EXAMPLES

```
 ENTER DEVICE NUMBER: SAMPLE7

                                                                    37

DEVICE UNDER TEST: MOTOROLA 3X3 1 MEGABIT BOARDS
LOT # A0123456-8
DATE: FEBRUARY 7,1984
TEMPERATURE: 25 DEGREES CELSIUS

BUBBLE MEMORY SYSTEM PRODUCTION TEST:
REVISION  2.00
MOTOROLA ENGINEERING RELEASE 1982

EXECUTING  50 INITIALIZATIONS
    SUCCESSFUL!!!!

EXECUTING MAP COMPARE TEST
    SUCCESSFUL!!!!

BUBBLE MEMORY DEVICE TYPE: MBM 2011  1M-BIT MEMORY
REDUNDANT LOOP NUMBERS:
 0000  0001  0002  0003  0004  0005  0006  0007  0008  0009
 0010  0013  0014  0016  0017  0018  0019  0020  0021  0022
 0024  0025  0026  0027  0029  0030  0031  0032  0033  0034
 0035  0043 *0051  0053  0054  0056  0063  0065  0074  0075
 0076  0085  0091  0101  0141  0192  0197 *0211  0212 *0232
*0283 *0292 *0370 *0374 *0375 *0376 *0392 *0569 *0580 *0581

* => NUMBER OF MASKED BAD LOOPS = 0013
    NUMBER OF MASKED WEAK LOOPS = 0047
TOTAL NUMBER OF REDUNDANT LOOPS = 0060

EXECUTING WRITE/READ TEST
 TEST PASS NUMBER = 0009
DATA PATTERN= $00  # PAGES = 0128
DATA PATTERN= $08  # PAGES = 0128
DATA PATTERN= $18  # PAGES = 0128
DATA PATTERN= $38  # PAGES = 0128
DATA PATTERN= $78  # PAGES = 0128
DATA PATTERN= $F8  # PAGES = 0128
DATA PATTERN= $F9  # PAGES = 0128
DATA PATTERN= $FB  # PAGES = 0128
DATA PATTERN= $FF  # PAGES = 0128
PSEUDO-RANDOM DATA # PAGES = 0896


**********************
PPP    AA    SS    SS
P  P  A  A  S   S  S   S
P  P  A  A  S      S
PPP   AAAA   SS    SS
P     A  A      S      S
P     A  A  S   S  S   S
P     A  A   SS    SS
**********************
```

* Successful completion of test sequence.

```
 TRY AGAIN? (Y/N) Y
  ENTER DEVICE NUMBER: SAMPLE3
```

38

```
DEVICE UNDER TEST: MOTOROLA 3X3 1 MEGABIT BOARDS
LOT # A0123456-8
DATE: FEBRUARY 7,1984
TEMPERATURE: 25 DEGREES CELSIUS

BUBBLE MEMORY SYSTEM PRODUCTION TEST:
REVISION  2.00
MOTOROLA ENGINEERING RELEASE 1982

EXECUTING  50 INITIALIZATIONS
    SUCCESSFUL!!!!

EXECUTING MAP COMPARE TEST
    SUCCESSFUL!!!!

BUBBLE MEMORY DEVICE TYPE: MBM 2011  1M-BIT MEMORY
REDUNDANT LOOP NUMBERS:
 0000  0001  0002  0003  0004  0005  0006  0007  0008  0009
 0010  0013  0014  0016  0017  0018  0019  0020  0021  0022
 0024  0025  0026  0027  0029  0030  0031  0032  0033  0034
 0035  0043 *0051  0053  0054  0056  0063  0065  0074  0075
 0076  0085  0091  0101  0141  0192  0197 *0211  0212 *0232
*0283 *0292 *0370 *0374 *0375 *0376 *0392 *0569 *0580 *0581

* => NUMBER OF MASKED BAD LOOPS = 0013
    NUMBER OF MASKED WEAK LOOPS = 0047
TOTAL NUMBER OF REDUNDANT LOOPS = 0060

EXECUTING WRITE/READ TEST
 TEST PASS NUMBER = 0005
DATA PATTERN= $00  # PAGES = 0128
DATA PATTERN= $02  # PAGES = 0128
DATA PATTERN= $06  # PAGES = 0128
DATA PATTERN= $0E  # PAGES = 0128
DATA PATTERN= $1E  # PAGES = 0128
DATA PATTERN= $3E  # PAGES = 0128
DATA PATTERN= $7E  # PAGES = 0128
DATA PATTERN= $FE  # PAGES = 0128
DATA PATTERN= $FF  # PAGES = 0128
PSEUDO-RANDOM DATA # PAGES = 0896
                                    READ DATA / EXPECTED DATA
*** ERROR: *** SAR= 00CC  STR= 09  LOOP# 0300 02 /02 0005 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0205  STR= 09  LOOP# 0294 3E /1E 0005 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 02F1  STR= 09  LOOP# 0458 7E /3E 0005 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 049A  STR= 09  LOOP# 0039 FF /7F 0005 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0627  STR= 09  LOOP# 0175 FC /DC 0005 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0627  STR= 09  LOOP# 0295 FF /EF 0005 ERROR TYPE: SOFT!

**********************
FFFF  AA  III L
F    A A   I  L
F    A A   I  L
FFF  AAAA  I  L
F    A A   I  L
F    A A   I  L
F    A A III LLLL
**********************
```

** DEVICE FAILS DUE TO SOFT ERRORS
(EXCESS-1 IMPLIES THRESHOLD TOO LOW)

```
ENTER DEVICE NUMBER: SAMPLE2

                                                                    39

DEVICE UNDER TEST: MOTOROLA 3X3 1 MEGABIT BOARDS
LOT # A0123456-8
DATE: FEBRUARY 7,1984
TEMPERATURE: 25 DEGREES CELSIUS

BUBBLE MEMORY SYSTEM PRODUCTION TEST:
REVISION  2.00
MOTOROLA ENGINEERING RELEASE 1982

EXECUTING  50 INITIALIZATIONS
* INITIALIZATION ERROR *
 STR= 21  @ ATTEMPT 00

*** MAP READ ERROR ***
MAP READ DATA:
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00

MAP READ DATA:
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00

**********************
FFFF  AA  III L
F    A A   I  L
F    A A   I  L
FFF  AAAA  I  L
F    A A   I  L
F    A A   I  L
F    A A III LLLL
**********************
```

** DEVICE FAILS FOR LACK OF MAPLOOP INFORMATION. THIS IS SOMETIMES THE RESULT OF IMPROPERLY INSERTED DEVICES.

```
  ENTER DEVICE NUMBER: SAMPLE5


DEVICE UNDER TEST: MOTOROLA 0X3 1 MEGABIT BOARDS
LOT # 00123456-8                                                    40
DATE: FEBRUARY 7,1984
TEMPERATURE: 25 DEGREES CELSIUS

BUBBLE MEMORY SYSTEM PRODUCTION TEST:
REVISION  2.00
MOTOROLA ENGINEERING RELEASE 1982

EXECUTING  50 INITIALIZATIONS
    SUCCESSFUL!!!!

EXECUTING MAP COMPARE TEST
    SUCCESSFUL!!!!

BUBBLE MEMORY DEVICE TYPE: MBM 2011  1M-BIT MEMORY
REDUNDANT LOOP NUMBERS:
 0000  0001  0002  0003  0004  0005  0006  0007  0008  0009
 0010  0013  0014  0016  0017  0018  0019  0020  0021  0022
 0024  0025  0026  0027  0029  0030  0031  0032  0033  0034
 0035  0043 *0051  0053  0054  0056  0063  0065  0074  0075
 0076  0085  0091  0101  0141  0192  0197 *0211  0212 *0232
*0283 *0292 *0370 *0374 *0375 *0376 *0392 *0569 *0580 *0581

* => NUMBER OF MASKED BAD LOOPS = 0013
     NUMBER OF MASKED WEAK LOOPS = 0047
TOTAL NUMBER OF REDUNDANT LOOPS = 0060

EXECUTING WRITE/READ TEST
 TEST PASS NUMBER = 0008
DATA PATTERN= $00   # PAGES = 0128
DATA PATTERN= $08   # PAGES = 0128
DATA PATTERN= $18   # PAGES = 0128
DATA PATTERN= $38   # PAGES = 0128
DATA PATTERN= $78   # PAGES = 0128
DATA PATTERN= $F8.  # PAGES = 0128
DATA PATTERN= $F9   # PAGES = 0128
DATA PATTERN= $FB   # PAGES = 0128
DATA PATTERN= $FF   # PAGES = 0128
PSEUDO-RANDOM DATA # PAGES = 0096
*** ERROR: *** SAR= 0080  STR= 09  LOOP# 0501 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0080  STR= 09  LOOP# 0533 00 /03 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0082  STR= 09  LOOP# 0270 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0082  STR= 09  LOOP# 0437 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0084  STR= 09  LOOP# 0145 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0084  STR= 09  LOOP# 0360 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0086  STR= 09  LOOP# 0380 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0086  STR= 09  LOOP# 0413 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0087  STR= 09  LOOP# 0028 00 /01 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0087  STR= 09  LOOP# 0485 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0093  STR= 09  LOOP# 0549 00 /01 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0094  STR= 09  LOOP# 0485 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0097  STR= 09  LOOP# 0161 00 /40 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0097  STR= 09  LOOP# 0221 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 0098  STR= 09  LOOP# 0535 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 009D  STR= 09  LOOP# 0120 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 00A1  STR= 09  LOOP# 0360 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 00A3  STR= 09  LOOP# 0429 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 00A6  STR= 09  LOOP# 0517 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 00A7  STR= 09  LOOP# 0477 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 00AA  STR= 09  LOOP# 0380 00 /08 0008 ERROR TYPE: HARD!
*** ERROR: *** SAR= 00AB  STR= 09  LOOP# 0296 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 00AB  STR= 09  LOOP# 0445 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 00AB  STR= 09  LOOP# 0541 00 /08 0008 ERROR TYPE: SOFT!
*** ERROR: *** SAR= 00AF  STR= 09  LOOP# 0112 00 /08 0008 ERROR TYPE: SOFT!

   MAXIMUM ERROR COUNT EXCEEDED

**********FAILED**********
FFFF  AA  III L
F    A A  I  L
F    A A  I  L
FFF  AAAA  I  L
F    A A  I  L
F    A A  I  L
F    A A III LLLL
**********FAILED**********
```

Maximum Error Count = 25
EXECUTION TERMINATED

** DEVICE FAILS FOR SOFT ERRORS
(EXCESS-0 IMPLIES THREHOLD
TOO HIGH)

```
TRY AGAIN? (Y/N) Y
  ENTER DEVICE NUMBER: SAMPLES

                                                                    41
DEVICE UNDER TEST: MOTOROLA 3X3 1 MEGABIT BOARDS
LOT # A01.23456-8
DATE: FEBRUARY 7, 1984
TEMPERATURE: 25 DEGREES CELSIUS

BUBBLE MEMORY SYSTEM PRODUCTION TEST:
REVISION  2.00
MOTOROLA ENGINEERING RELEASE 1982

EXECUTING  50 INITIALIZATIONS
* INITIALIZATION ERROR *
 STR= 09  @ ATTEMPT 00

MAP READ DATA:
00 19 01 08 0F EF E9 7E BF C7 FB EF FB FF FF FF FF FB FF FF FF FF FF FF 7B
FF E7 FF FF 7F FF FF FF FF FF EF F7 FF FF FF FF FF FF FF FF FF FF DC 7F FF 7F
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF BF F3 52 29
12 86 04 9E 01 CB FF FF FF FD FF FA 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 02

MAP READ DATA:
00 19 01 08 0F EF E9 7E BF C7 FB EF FB FF FF FF FF FB FF FF FF FF FF FF 7B
FF E7 FF FF 7F FF FF FF FF FF EF F7 FF FF FF FF FF FF FF FF FF FF DC 7F FF 7F
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF BF F3 52 29
12 86 04 9E 01 CB FF FF FF FD FF FA 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 02


**********************
FFFF   AA   III L
F     A  A   I  L
F     A  A   I  L
FFF   AAAA   I  L
F     A  A   I  L
F     A  A   I  L
F     A  A III LLLL
**********************
```

** DEVICE FAILS FOR ERROR IN MAPLOOP INFORMATION.

MAPLOOP CONTENTS ARE DISPLAYED.

```
TRY AGAIN? (Y/N) Y
 ENTER DEVICE NUMBER: SAMPLE1
```

42

```
DEVICE UNDER TEST: MOTOROLA 3X3 1 MEGABIT BOARDS
LOT # A0123456-8
DATE: FEBRUARY 7,1984
TEMPERATURE: 25 DEGREES CELSIUS

BUBBLE MEMORY SYSTEM PRODUCTION TEST:
REVISION  2.00
MOTOROLA ENGINEERING RELEASE 1982

EXECUTING  50 INITIALIZATIONS
    SUCCESSFUL!!!!

EXECUTING MAP COMPARE TEST
    SUCCESSFUL!!!!

BUBBLE MEMORY DEVICE TYPE: MBM 2011  1M-BIT MEMORY
REDUNDANT LOOP NUMBERS:
 0000  0001  0002  0003  0004  0005  0006  0007  0008  0009
 0010  0013  0014  0016  0017  0018  0019  0020  0021  0022
 0024  0025  0026  0027  0029  0030  0031  0032  0033  0034
 0035  0043 *0051  0053  0054  0056  0063  0065  0074  0075
 0076  0085  0091  0101  0141  0192  0197 *0211  0212 *0232
*0283 *0292 *0370 *0374 *0375 *0376 *0392 *0569 *0580 *0581

* => NUMBER OF MASKED BAD LOOPS = 0013
    NUMBER OF MASKED WEAK LOOPS = 0047
TOTAL NUMBER OF REDUNDANT LOOPS = 0060

EXECUTING WRITE/READ TEST
 TEST PASS NUMBER = 0003
DATA PATTERN= $00  # PAGES = 0128
DATA PATTERN= $02  # PAGES = 0128
DATA PATTERN= $06  # PAGES = 0128
DATA PATTERN= $0E  # PAGES = 0128
DATA PATTERN= $1E  # PAGES = 0128
DATA PATTERN= $3E  # PAGES = 0128
DATA PATTERN= $7E  # PAGES = 0128
DATA PATTERN= $FE  # PAGES = 0128
DATA PATTERN= $FF  # PAGES = 0128
PSEUDO-RANDOM DATA # PAGES = 0896
*** ERROR:  *** SAR= 01E3  STR= 09  LOOP# 0359 1E /0E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0232  STR= 09  LOOP# 0151 3E /1E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0238  STR= 09  LOOP# 0244 3E /1E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 029F  STR= 09  LOOP# 0442 7E /3E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 02A0  STR= 09  LOOP# 0402 7E /3E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 031D  STR= 09  LOOP# 0116 FE /7E 0003 ERROR TYPE:  HARD!
*** ERROR:  *** SAR= 031D  STR= 09  LOOP# 0132 FE /7E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0345  STR= 09  LOOP# 0049 FE /7E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0345  STR= 09  LOOP# 0081 FE /7E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 036F  STR= 09  LOOP# 0124 FE /7E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 036F  STR= 09  LOOP# 0132 FE /7E 0003 ERROR TYPE:  HARD!
*** ERROR:  *** SAR= 036F  STR= 09  LOOP# 0274 FE /7E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0487  STR= 09  LOOP# 0221 BD /BC 0003 ERROR TYPE:  HARD!
*** ERROR:  *** SAR= 0487  STR= 09  LOOP# 0243 F6 /B6 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0488  STR= 09  LOOP# 0503 BB /B9 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 04B8  STR= 09  LOOP# 0516 FE /7E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 04D8  STR= 09  LOOP# 0306 9F /9F 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 04E8  STR= 09  LOOP# 0200 FE /7E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 04E8  STR= 09  LOOP# 0217 FF /7F 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0501  STR= 09  LOOP# 0347 FD /FC 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0501  STR= 09  LOOP# 0355 FF /FE 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0547  STR= 09  LOOP# 0122 77 /75 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0547  STR= 09  LOOP# 0303 9F /9E 0003 ERROR TYPE:  SOFT!
*** ERROR:  *** SAR= 0584  STR= 09  LOOP# 0093 DF /DE 0003 ERROR TYPE:  HARD!
*** ERROR:  *** SAR= 0584  STR= 09  LOOP# 0121 FF /FE 0003 ERROR TYPE:  SOFT!

   MAXIMUM ERROR COUNT EXCEEDED

FFFF  AA  III L
F    A A   I  L
F    A A   I  L
FFF  AAA   I  L
F    A A   I  L
F    A A   I  L
F    A A  III LLLL
```

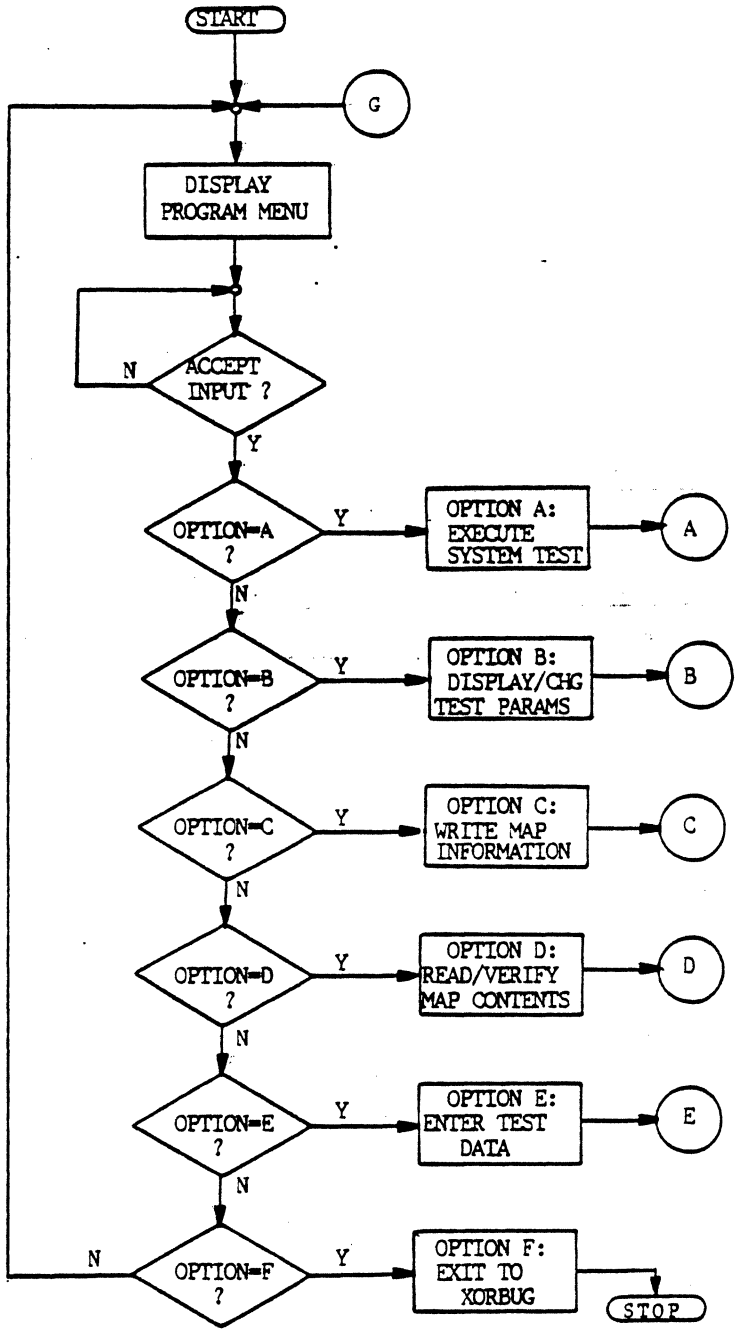
NOTE: WHEN SOFT ERRORS ARE VERY FREQUENT, THEY MAY REGISTER AS HARD ERRORS.

Maximum Error Count = 25
EXECUTION TERMINATED

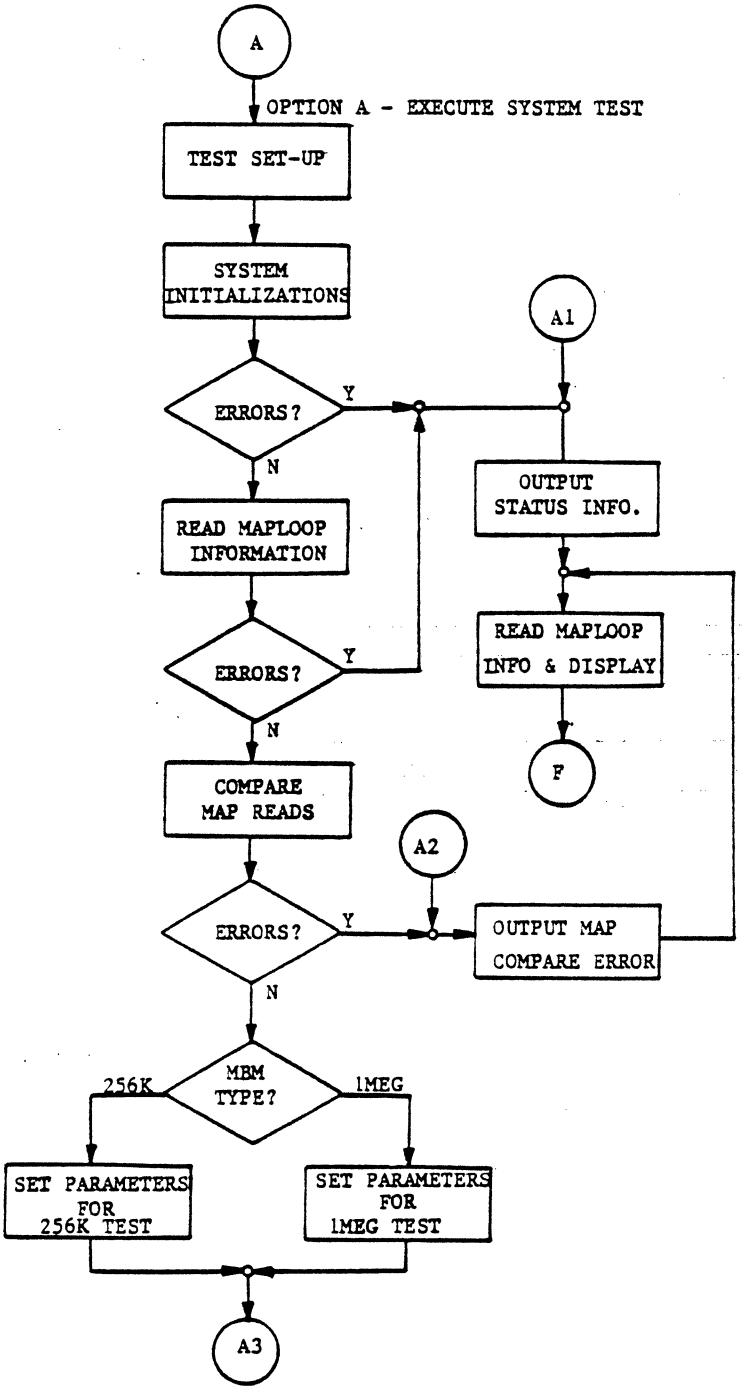
** DEVICE FAILS FOR SOFT ERRORS.
(EXCESS-1 IMPLIES THRESHOLD TOO LOW)

CHAPTER 6
BUBLTEST SOFTWARE FLOWCHARTS

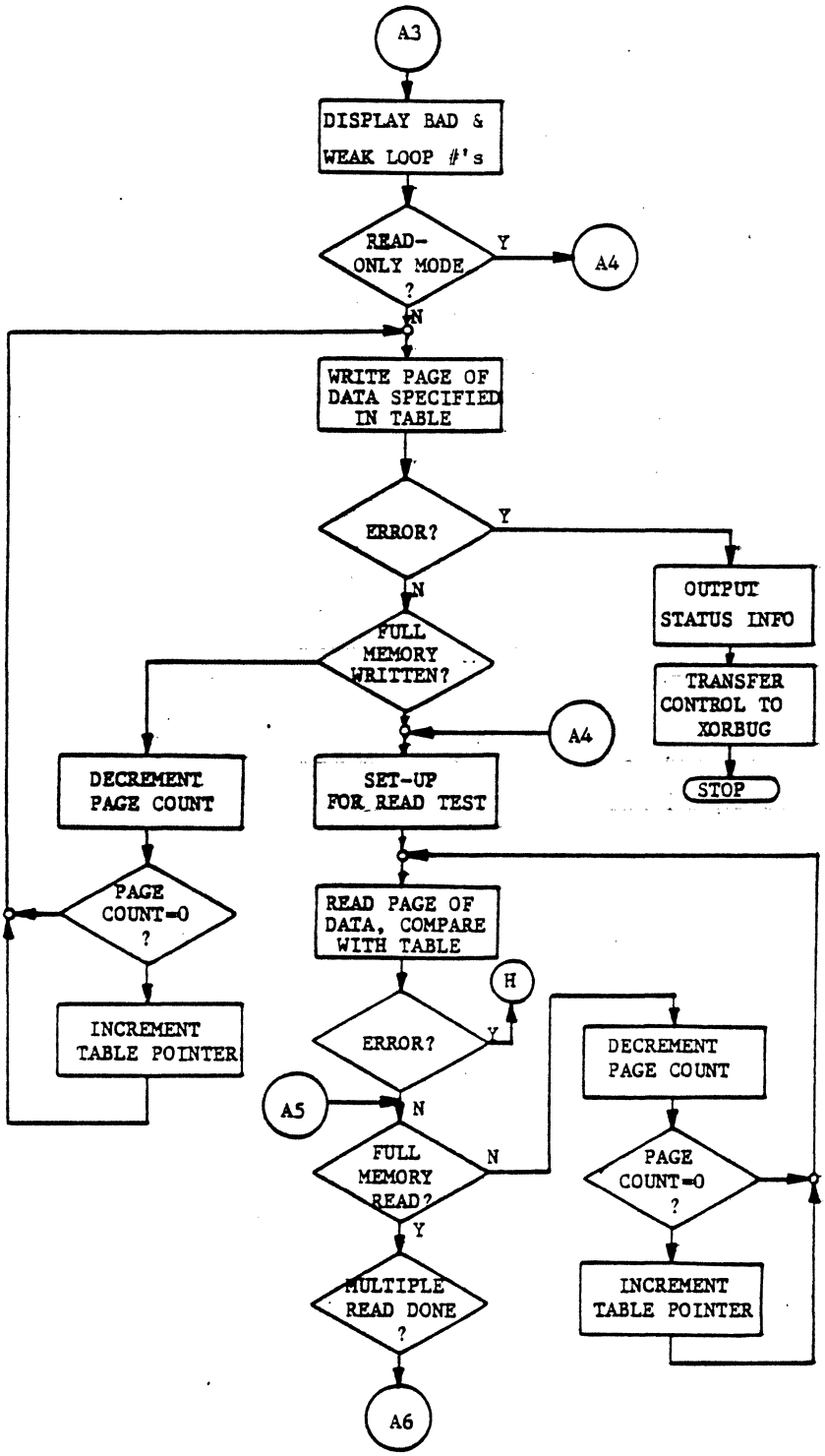
BUBLTEST MAIN PROGRAM MENU 44



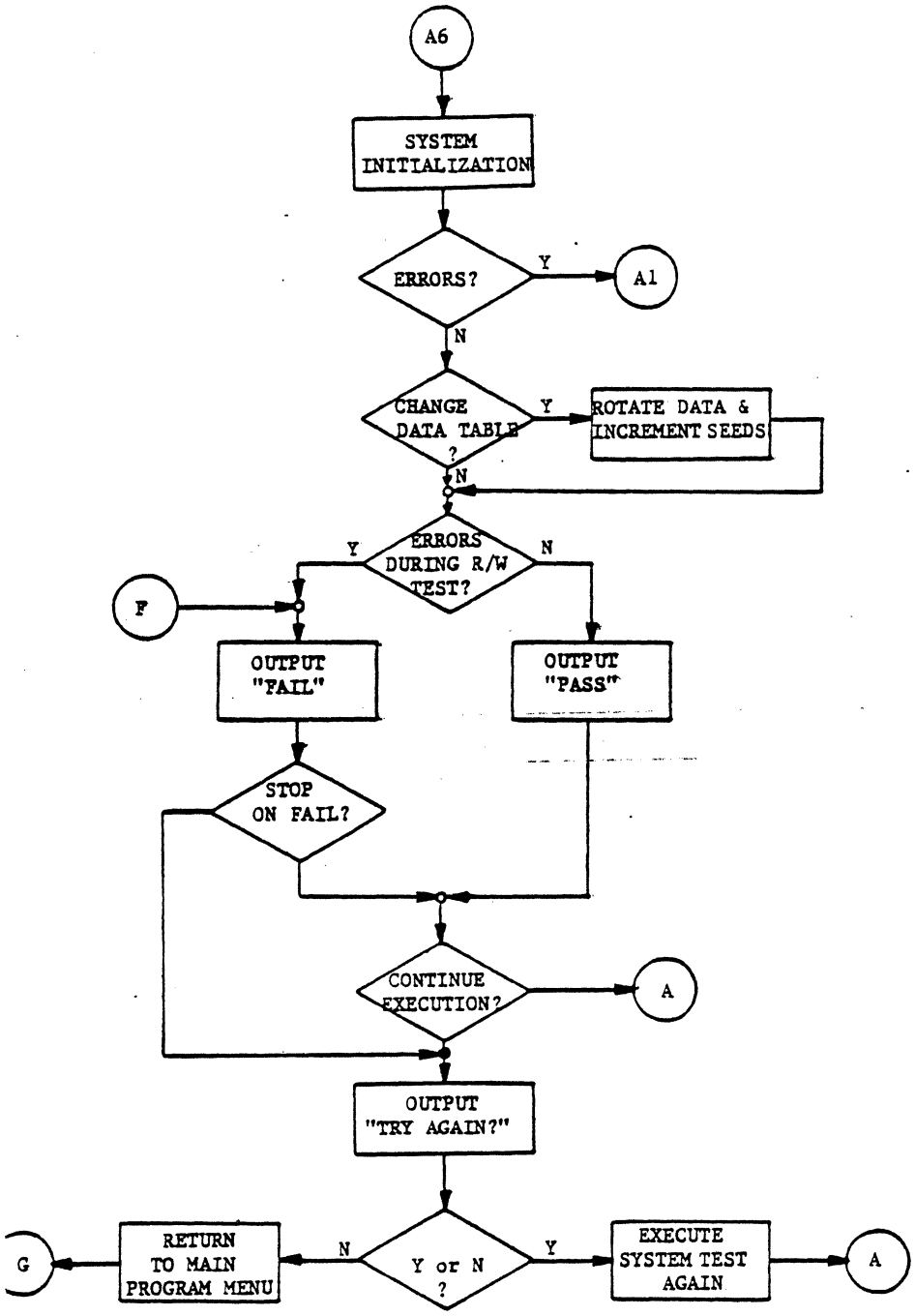
45

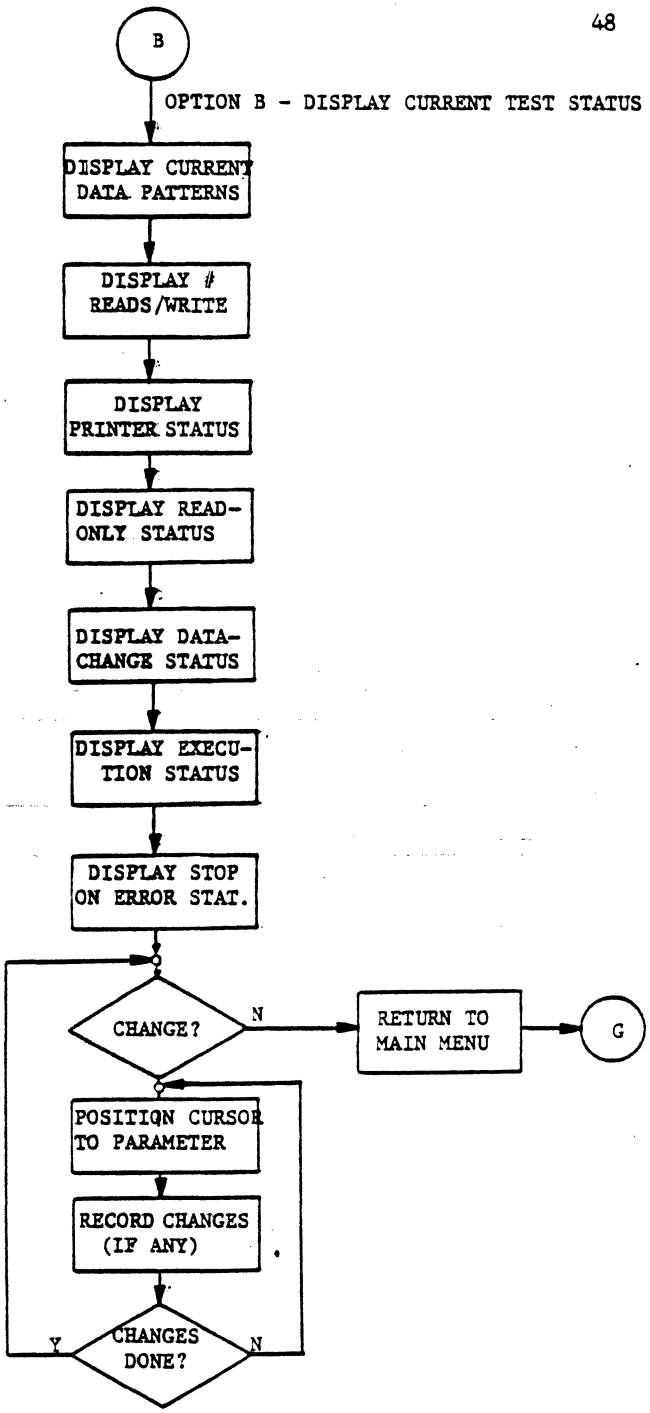

A
OPTION A - EXECUTE SYSTEM TEST
TEST SET-UP
SYSTEM INITIALIZATIONS
A1
ERRORS?
Y
N
OUTPUT STATUS INFO.
READ MAPLOOP INFORMATION
READ MAPLOOP INFO & DISPLAY
ERRORS?
Y
N
F
COMPARE MAP READS
A2
ERRORS?
Y
OUTPUT MAP COMPARE ERROR
N
MBM TYPE?
256K
1MEG
SET PARAMETERS FOR 256K TEST
SET PARAMETERS FOR 1MEG TEST
A3

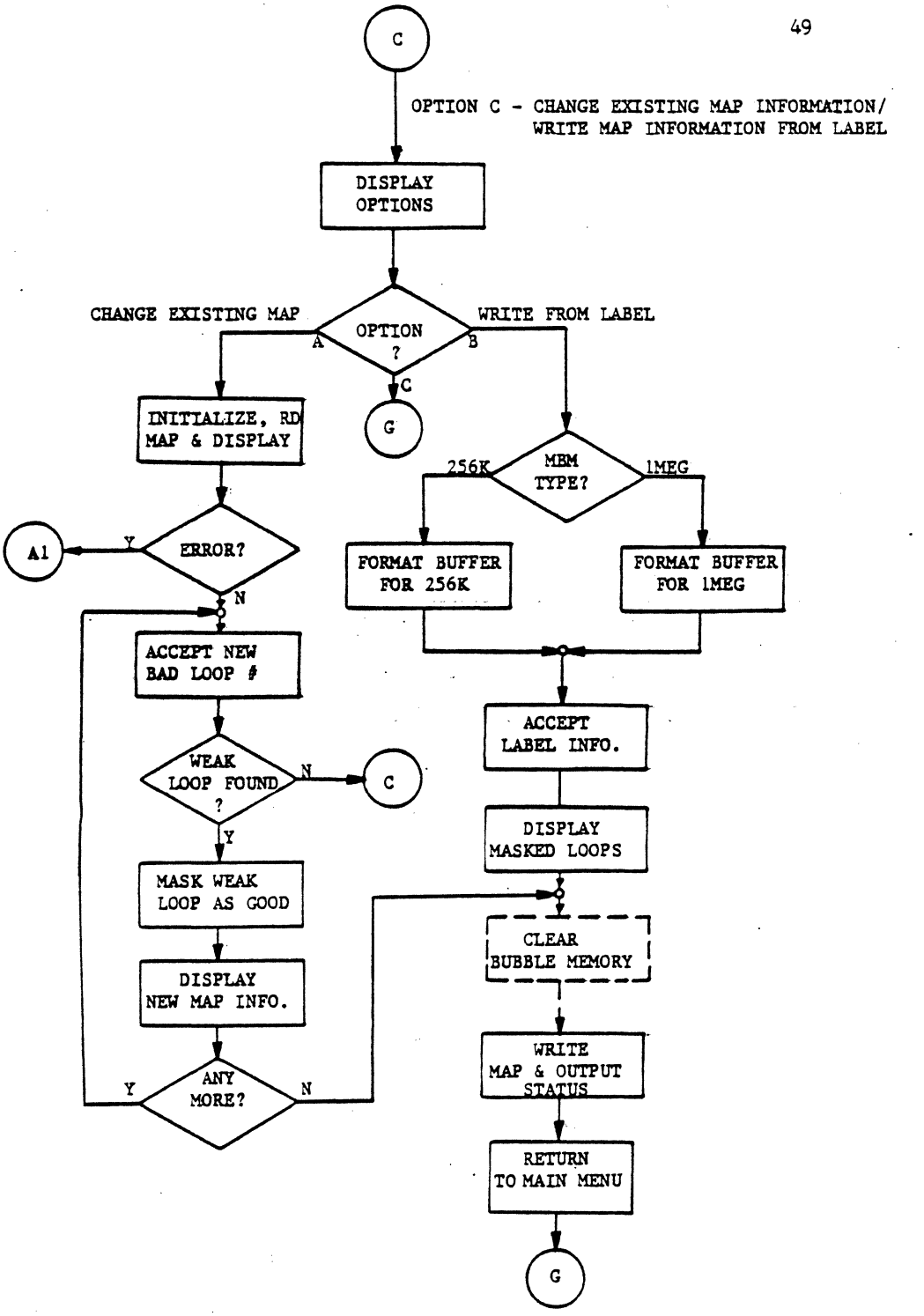
46

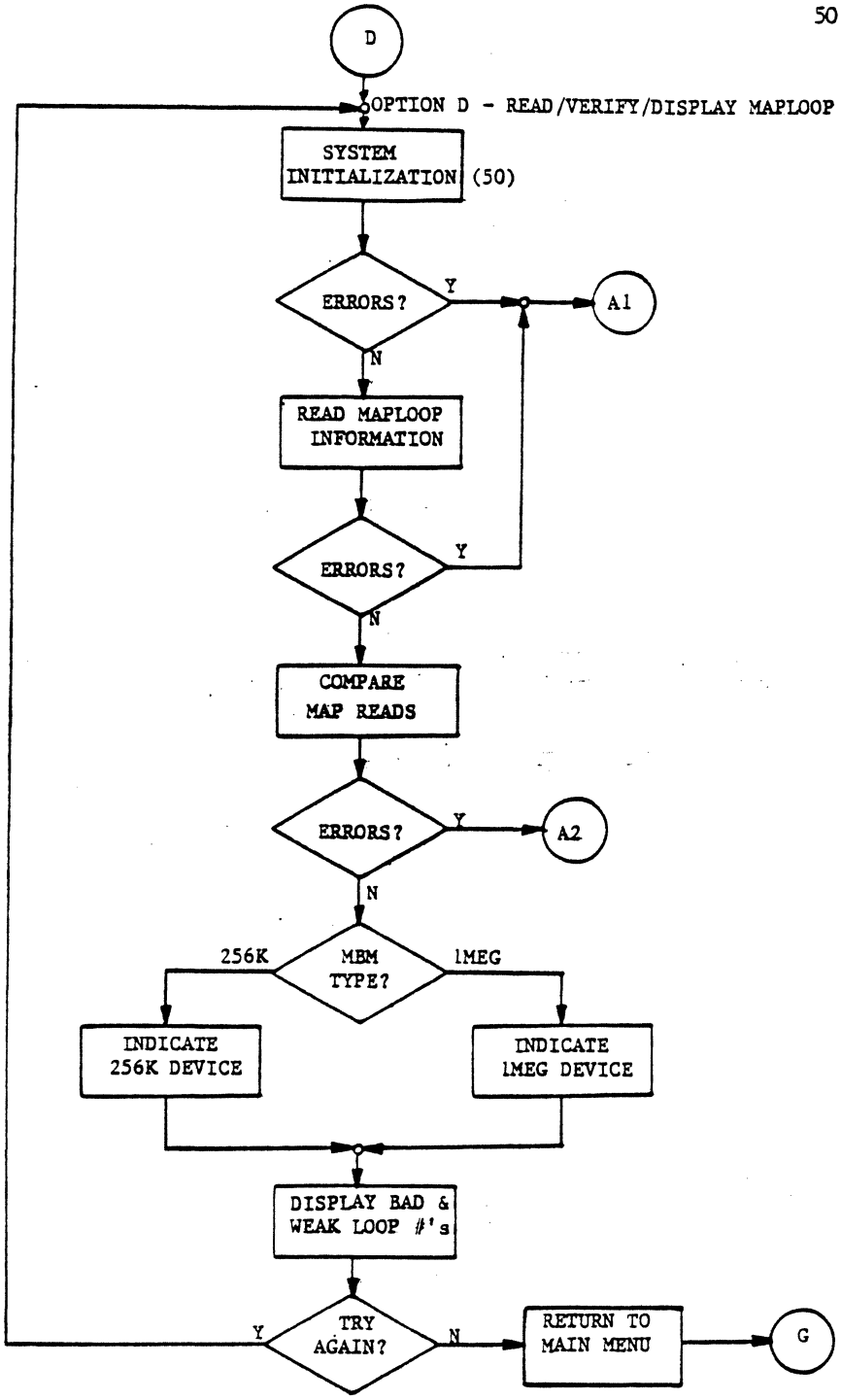

A3
DISPLAY BAD & WEAK LOOP #'s
READ-ONLY MODE ?
Y
A4
N
WRITE PAGE OF DATA SPECIFIED IN TABLE
ERROR?
Y
OUTPUT STATUS INFO
TRANSFER CONTROL TO XORBUG
STOP
N
FULL MEMORY WRITTEN?
A4
DECREMENT PAGE COUNT
SET-UP FOR READ TEST
PAGE COUNT=0 ?
READ PAGE OF DATA, COMPARE WITH TABLE
H
INCREMENT TABLE POINTER
ERROR?
Y
A5
N
DECREMENT PAGE COUNT
FULL MEMORY READ?
N
PAGE COUNT=0 ?
Y
MULTIPLE READ DONE ?
INCREMENT TABLE POINTER
A6

47

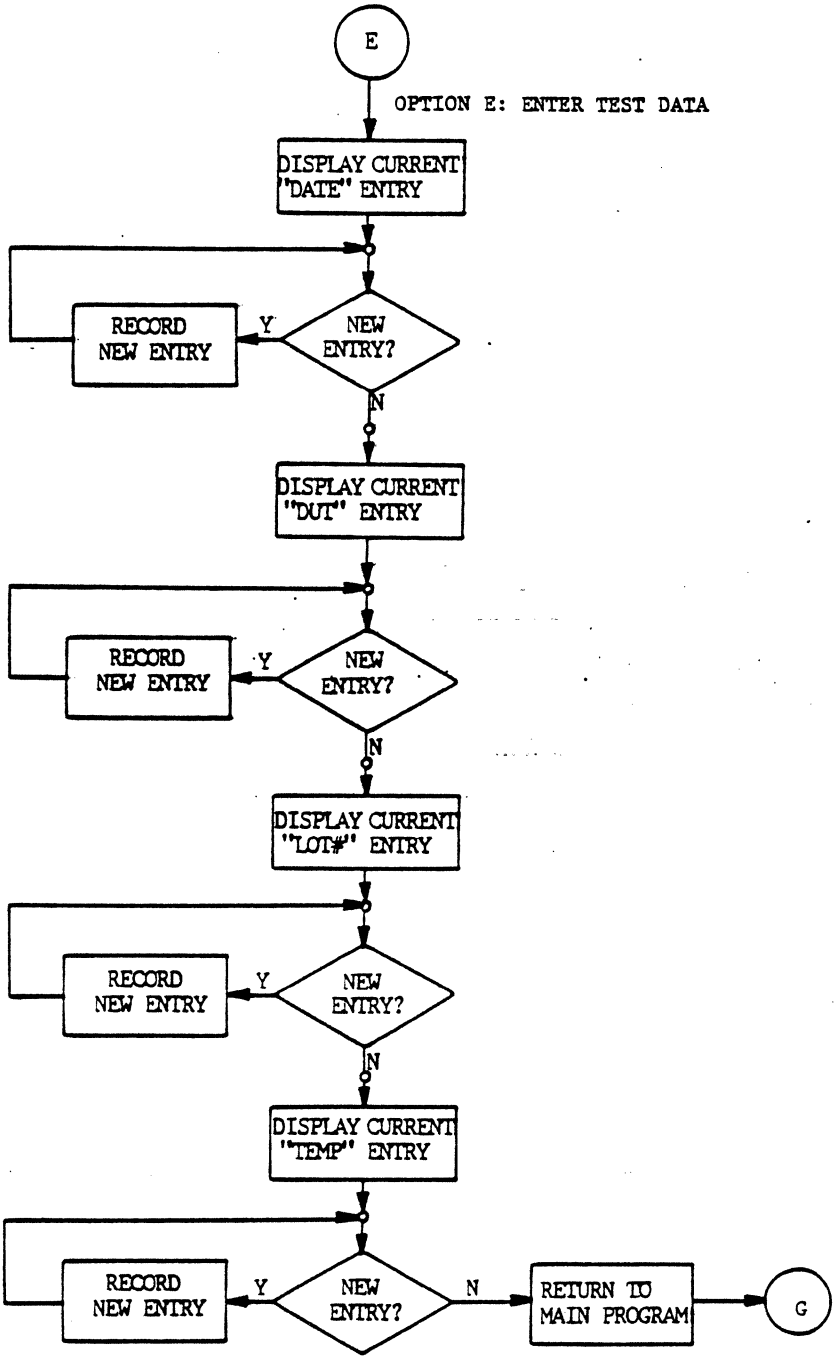

A6
SYSTEM INITIALIZATION
ERRORS?
Y
A1
N
CHANGE DATA TABLE ?
Y
ROTATE DATA & INCREMENT SEEDS
N
ERRORS DURING R/W TEST?
Y
N
F
OUTPUT "FAIL"
OUTPUT "PASS"
STOP ON FAIL?
CONTINUE EXECUTION?
A
OUTPUT "TRY AGAIN?"
G
RETURN TO MAIN PROGRAM MENU
N
Y or N ?
Y
EXECUTE SYSTEM TEST AGAIN
A


48
B
OPTION B - DISPLAY CURRENT TEST STATUS
DISPLAY CURRENT DATA PATTERNS
DISPLAY # READS/WRITE
DISPLAY PRINTER STATUS
DISPLAY READ-ONLY STATUS
DISPLAY DATA-CHANGE STATUS
DISPLAY EXECU-TION STATUS
DISPLAY STOP ON ERROR STAT.
CHANGE?
N
RETURN TO MAIN MENU
G
POSITION CURSOR TO PARAMETER
RECORD CHANGES (IF ANY)
CHANGES DONE?
Y
N

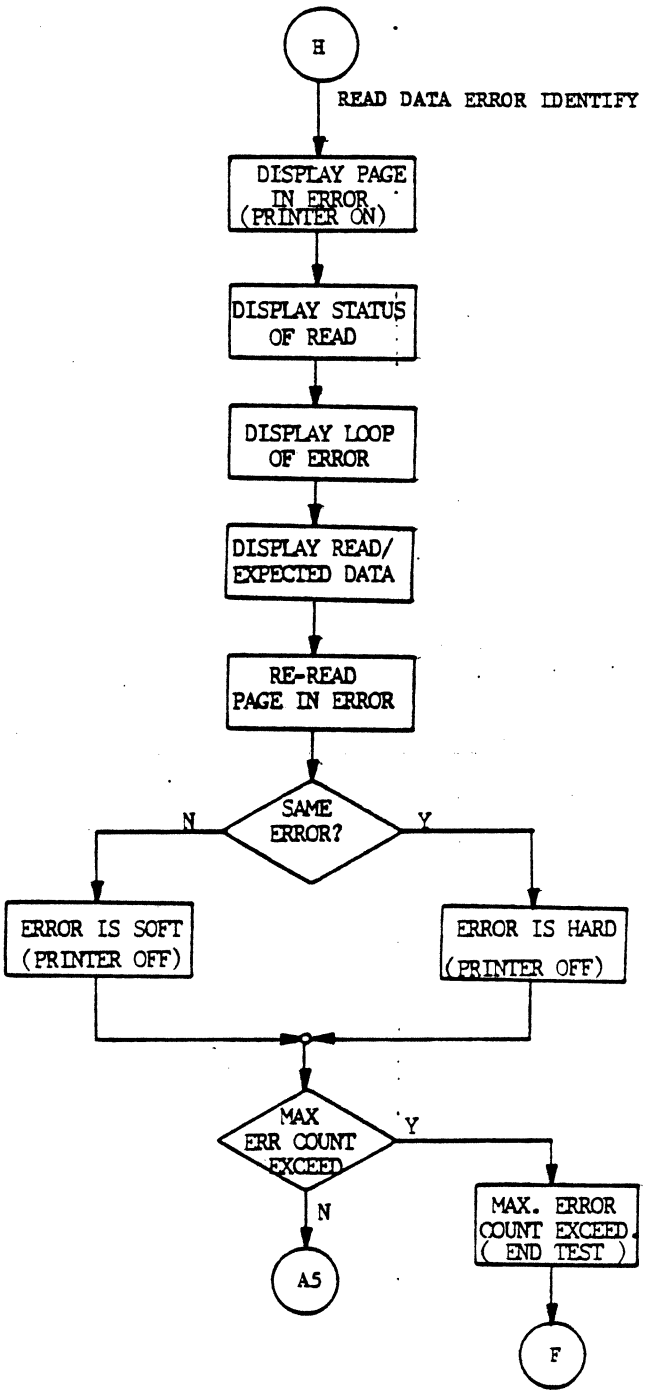

C
OPTION C - CHANGE EXISTING MAP INFORMATION/
WRITE MAP INFORMATION FROM LABEL
DISPLAY OPTIONS
CHANGE EXISTING MAP
OPTION ?
WRITE FROM LABEL
A
B
C
INITIALIZE, RD MAP & DISPLAY
G
256K
MEM TYPE?
1MEG
A1
Y
ERROR?
FORMAT BUFFER FOR 256K
FORMAT BUFFER FOR 1MEG
N
ACCEPT NEW BAD LOOP #
ACCEPT LABEL INFO.
WEAK LOOP FOUND ?
N
C
DISPLAY MASKED LOOPS
Y
MASK WEAK LOOP AS GOOD
CLEAR BUBBLE MEMORY
DISPLAY NEW MAP INFO.
WRITE MAP & OUTPUT STATUS
Y
ANY MORE?
N
RETURN TO MAIN MENU
G


50
D
OPTION D - READ/VERIFY/DISPLAY MAPLOOP CONTENTS
SYSTEM INITIALIZATION (50)
ERRORS?
Y
A1
N
READ MAPLOOP INFORMATION
ERRORS?
Y
N
COMPARE MAP READS
ERRORS?
Y
A2
N
256K
MEM TYPE?
1MEG
INDICATE 256K DEVICE
INDICATE 1MEG DEVICE
DISPLAY BAD & WEAK LOOP #'s
Y
TRY AGAIN?
N
RETURN TO MAIN MENU
G

51


E
OPTION E: ENTER TEST DATA
DISPLAY CURRENT "DATE" ENTRY
NEW ENTRY?
Y
RECORD NEW ENTRY
N
DISPLAY CURRENT "DUT" ENTRY
NEW ENTRY?
Y
RECORD NEW ENTRY
N
DISPLAY CURRENT "LOT#" ENTRY
NEW ENTRY?
Y
RECORD NEW ENTRY
N
DISPLAY CURRENT "TEMP" ENTRY
NEW ENTRY?
Y
RECORD NEW ENTRY
N
RETURN TO MAIN PROGRAM
G

52


H
READ DATA ERROR IDENTIFY
DISPLAY PAGE IN ERROR (PRINTER ON)
DISPLAY STATUS OF READ
DISPLAY LOOP OF ERROR
DISPLAY READ/ EXPECTED DATA
RE-READ PAGE IN ERROR
SAME ERROR?
N
Y
ERROR IS SOFT (PRINTER OFF)
ERROR IS HARD (PRINTER OFF)
MAX ERR COUNT EXCEED
Y
N
MAX. ERROR COUNT EXCEED (END TEST)
A5
F

CHAPTER 7

BUBLTEST SOURCE CODE LISTING

```
IBLTEST.SA:1        BUBBLE MEMORY SYSTEM TEST PROGRAM:

       OPT    LLE=95
**********************************************************
**********************************************************
**                                                      **
**         256K- AND 1M-BIT                             **
**   BUBBLE MEMORY SYSTEM                               **
**          TEST PROGRAM                                **
**                                                      **
**   REVISION 2.00                                      **
**                                                      **
**   DATE: 11/18/82                                     **
**                                                      **
**   WRITTEN BY: RICK BRZOZOWY                          **
**               MICARL SYSTEMS DESIGN AND              **
**               DEVELOPMENT                            **
**                                                      **
**            BUBLTEST                                  **
**********************************************************
**********************************************************
*
       TTL    ** PROGRAM REVISION TABLE **
```

NOTE: The BUBLTEST source code listing is not included as part of this manuscript.

APPENDIX B

DATA SHEETS

MOTOROLA

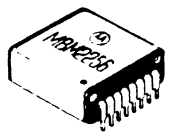
BUBBLE MEMORY PRODUCTS

7402 SOUTH PRICE ROAD • TEMPE, ARIZONA 85283

MBM2256

Advance Information

256 K x 1-BIT MAGNETIC BUBBLE MEMORY DEVICE



GENERAL DESCRIPTION

The MBM2256 is a 262,144 (2^{18}) bit magnetic bubble memory device. All required magnetic components including the permanent magnets, the drive field coils and protective magnetic shield are integral parts of the device. The package is a 1.15 x 1.1 x 0.36 inch 16-pin DIP.

The MBM2256 features a dual block-replicate organization with swap gates on the input track. Data storage is organized as 256 storage loops of 1024-bits each. Additional loops are provided to store the error correction code and as redundant loops. In one of two dedicated map loops on-chip the redundant map loop data is stored.

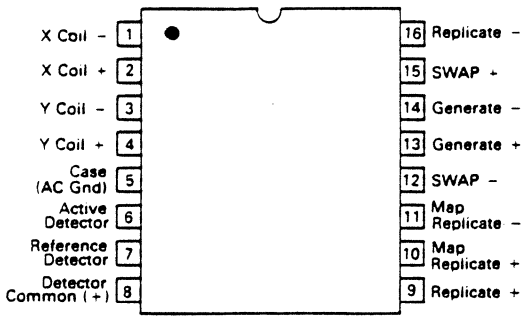
The MBM2256 can be operated synchronously or asynchronously. Average access time to a page of data is less than 7.0 ms at 100 kHz. Data transfer rate is 125 kilobits per second at 125 kHz. Average power dissipation at 125 kHz is 0.8 Watts. The device will operate over a case temperature range of 0°C to 70°C, and data is retained without power from −40°C to 100°C.

The device is fabricated using a pseudo-planar process to improve operating margins as well as to enhance reliability. The use of CrCuCr in the conductor elements ensures excellent conductivity while greatly increasing resistance to problems associated with electromigration.

FEATURES

- Non-volatile
- High Density
- Solid State
- Low Power
- Start/Stop Capability
- Page-Oriented Access
- On-Chip Redundant Loop Map
- Swap Gates
- Block Replicate
- Error Correction Code Storage
- 16-Pin Dual-in-Line Package

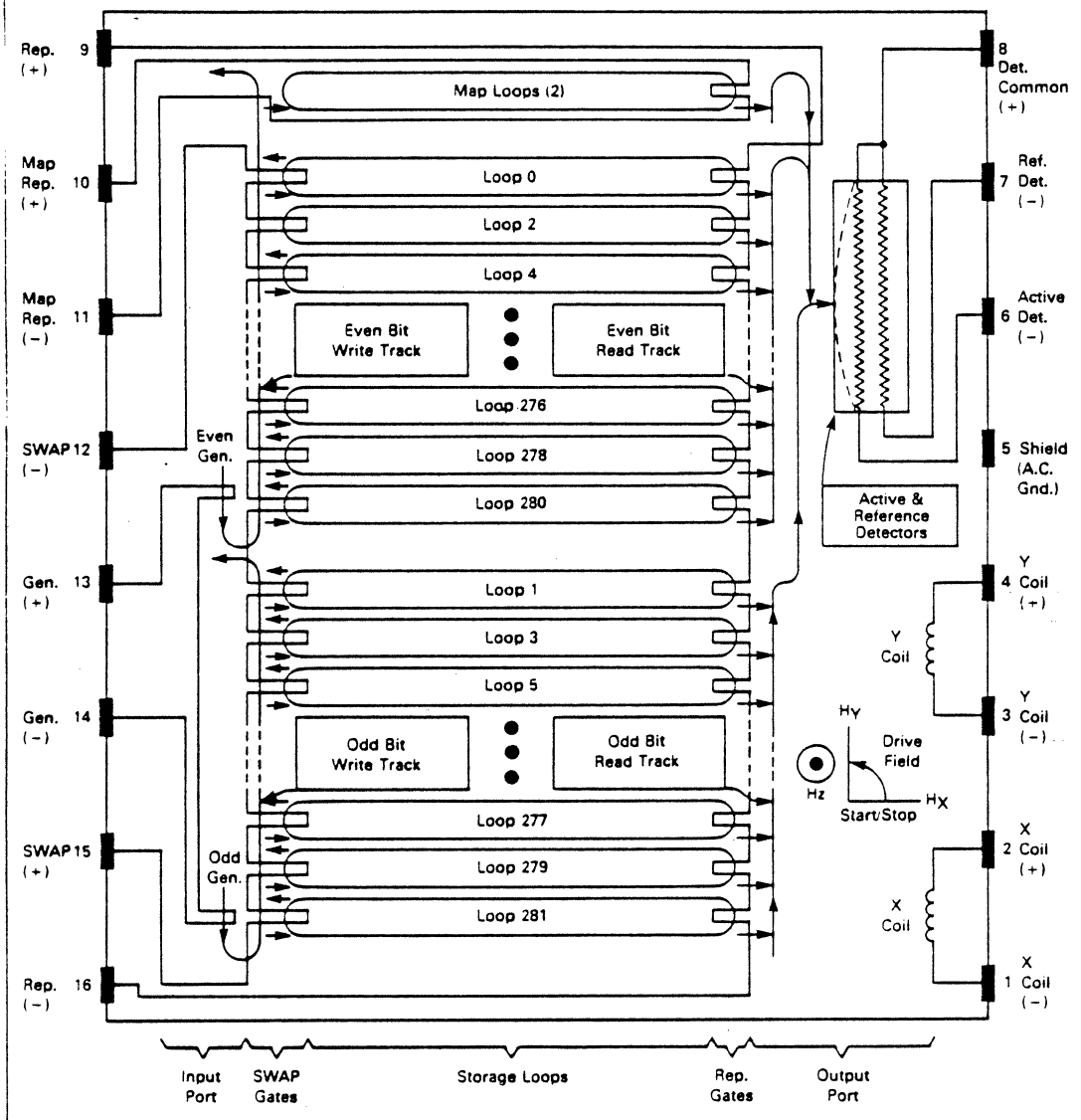
Pin Assignment



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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FIGURE 1 — BLOCK DIAGRAM



*NOTE:
The (+) jack for the Z coil is the one closest to Pin 8.

ABSOLUTE MAXIMUM RATINGS

Rating	Min	Max	Unit
Operating Temperature (Case) (T_C)	0	70	°C
Non-Volatile Storage Temperature	-40	100	°C
Storage Temperature	-40	120	°C
External Magnetic Field	—	20	Oe
Peak Current In X Coil*	—	900	mA
Peak Current In Y Coil*	—	1,100	mA
Peak Current In Z Coil*	—	3,000	mAdc
Peak Replicate Current	—	40	mAdc
Peak Generate Current	—	40	mAdc
Peak Swap Current	—	30	mAdc
Peak Detector Current	—	6.0	mAdc
Maximum Coil Disturb Current With Data Retention	—	10	mA
Maximum Pin To Pin Voltage	—	55	Volts

*These peak currents are allowed subject to the device temperature not exceeding the temperature limits.

ELECTRICAL CHARACTERISTICS (T_C = 0°C to 70°C, rotating field frequency (f_o) = 125 kHz unless otherwise noted).

FUNCTION CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Generate Current	I_G	180	—	220	mA
Swap Current	I_S	25	—	31	mA
Replicate Cut Current	I_{RC}	75	—	95	mA
Replicate Transfer Current	I_{RT}	28	—	42	mA
Map Replicate Cut Current	I_{RCM}	75	—	95	mA
Map Replicate Transfer Current	I_{RTM}	28	—	42	mA
Map Transfer In Current	I_{TM}	-24	—	-30	mA
Detector Current	I_{DA}, I_{DR}	—	5.0	5.8	mA

X,Y COIL DRIVE (See Figure 2.)

Parameter	Symbol	Min	Typ	Max	Unit
Coil Driver Supply Voltage	V_x, V_y	11.4	12	12.6	V
Coil Driver Switch On Resistance (2 Switches In Series)	R_{on}	0.7	—	1.8	Ohms
Coil Driver Clamp Diode Drop (2 Diodes In Series)	V_{clamp}	—	—	1.6	V
X Coil Peak Current (L_x = nom, V_x = nom, R_{on}, V_{clamp} = nom)	I_{XP}	—	630	—	mA
Y Coil Peak Current (L_y = nom, V_y = nom) (R_{on}, V_{clamp} = nom)	I_{YP}	—	770	—	mA
Coil Current Offset	I_{xo}, I_{yo}	-10	—	+10	mA
Stop Current Overshoot	I_{so}	—	—	+10 -0	mA
Total Coil Power	P_c	—	—	1.0	W

Z COIL DRIVE

Z Coil Sensitivity		—	26.5	—	Oe/A
Z Coil Current Simultaneously Erase All Data Stored (Rotating Field On) (Rotating Field Off)	I_{zap}	 2.0 3.0	 — —	 — —	A
Duration of Erase Current	t_{ZAP}	0.5	—	10	ms

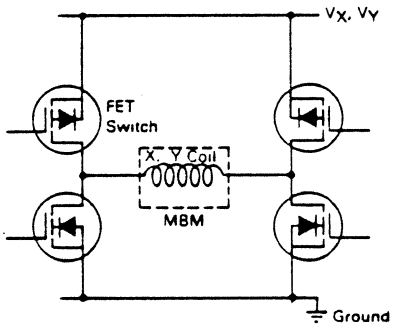
SCOPE

This specification describes the magnetic, electrical, mechanical and environmental parameters of the 256K bit magnetic bubble device, MBM2256, as manufactured by Motorola Inc.

DEVICE ORGANIZATION

The 256K bit bubble memory chip uses a block-replicate organization with true swap gates on the input track. The storage area is arranged as 256 storage loops each with 1,024 bit locations. Additional loops are provided for error correction (6) and defect tolerance (20) giving a total of 282 loops. Data is written and read at the clock frequency which is the rotating field frequency. Figure 1 is a schematic diagram of the 256K bit chip.

FIGURE 2 — X, Y COIL DRIVE



(a.) TYPICAL DRIVE CIRCUIT

Data Input

The device is organized into two halves — odd and even. To write into the device the same data pattern is written simultaneously into both the odd and even input tracks. Due to the spacing between minor loops only alternate bits can be aligned with adjacent minor loops. An extra bit propagation delay on the odd input track causes odd bits to align with odd loops and even bits with even loops such that the correct bit is written into each loop. The swap gate automatically clears the old data as new data is written into the loops.

Data Output

To read the data, one bit is replicated from each minor loop into the output track, again arranged as an odd and even half. The alternate bit data streams are then interleaved prior to entering the detector. The data is therefore written in and read out of the bubble device at the clock frequency although the data does divide and recombine within the chip.

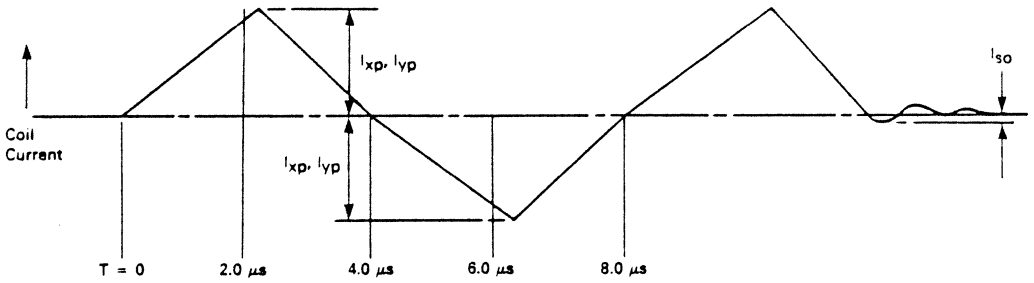
Redundancy

Of the 282 storage loops 256 are allocated for data, 6 for error correction and 20 for redundancy. These 20 loops are used to mask inoperable minor loops and improve performance. Twenty loops are always declared redundant. Data should not be written into the redundant loops.

Redundancy Map

In addition to the 282 storage loops the chip contains two map loops. These loops have their own transfer-in and replicate gates but share the generator and detector with the storage loops. Only one loop is required and is chosen at final test. The chosen loop is used to store the data which identifies the redundant loop map. A "one" designates a usable loop; a "zero" a non-usable loop. Preceding this map code is a stream of 64 "zeros" followed by a "one" and a "zero" which may be used to synchronize the external control circuitry with the memory. The map loop used for storage of the redundancy information is also identified in the code (see Coding of Redundancy Map). Since only alternate bit positions are written into the map loop to enhance reliability, intervening bits are always zero and are ignored during read (see Map Read Operation paragraph).

The redundancy map is also printed on the label of each device using hexadecimal format. Two digits are used per loop. Instead of providing the absolute loop number, the incremental difference between non-usable loops is printed. For example, if the first bad loop is #7, and the next two are 19 and 23, the sequence



(b.) TYPICAL RISE/FALL IMBALANCE DUE TO DRIVE CIRCUIT

070C04 will be printed on the label. This format allows for an incremental difference between two non-usable loops of up to 255 (FF).

Coding of Redundancy Map (The map loop contains 512 bits of information in five fields.)

Pattern	Field	Number of Bits	Note
MM---MM	Map Data	282	(1)
EE---EE	Error Correction	12	(2)
LL	Loop	2	(3)
UU---UU	User	150	(4)
00---0010	Sync	66	(5)

NOTE:
(1) Each bit corresponds to a data loop in sequence
M = 1 identifies a usable loop (262).
M = 0 identifies a redundant loop (20).
(2) Error correction code used is a fire code applied only to the map data.
(3) Identifies which map loop contains the redundancy information
01 — loop #1, 10 — loop #2.
(4) This field may contain factory-pertinent information. It will not contain a duplicate of the sync pattern.
(5) The sync pattern is used to locate the beginning of the map data field and identifies data page zero.

Organizational Specifications

Bits/Loop	1,024
Total Data Loops	282
Usable Data Loops	262
Error Correction Loops	6
User Data Loops	256
Total User Storage	262,144 Bits
Map Loops	2

FUNCTIONAL DESCRIPTION

Write Data Operation

Writing data is accomplished by generating the new data with a series of pulses applied to pins 13 and 14, starting t_{PGSF} before the swap operation. As the device continues to cycle after all data is generated, the new data and the old will be aligned at the swap gates after t_{PGSL}. A swap pulse is applied to pins 12 and 15 at this time, swapping the new data in and the old data out. Unused bits from the even and odd sides along with the old data are propagated out and discarded beyond the active area.

Read Data Operation

To read data, the device must be cycled until the desired page is aligned with the replicate gates on the output side of the storage loops. A replicate cut pulse is applied to pins 9 and 16 to duplicate the page. This is immediately followed by a replicate transfer pulse which causes the duplicate bubbles to propagate into alternate positions on the two output tracks.

Propagation along the output tracks occurs during t_{PRD}. During this time, the odd and even output bits are merged.

Detection occurs when a bubble passes under the magnetoresistive detector element. The bubble's magnetic field causes the detector element to change resistance. By passing a constant current through the detector, this is converted to a voltage signal. A dummy detector which is not influenced by magnetic bubbles is used to cancel the background magnetoresistive signal.

Output bubbles are discarded beyond the active area after detection. A complete page is read in t_{PRDL}.

INTERFACE IMPEDANCES

Parameter	Symbol	Min	Typ	Max	Unit
Generate (1)	r_G	4.5	—	18	Ω
Swap (1)	r_S	180	—	540	Ω
Replicate (1)	r_R	130	—	320	Ω
Map Replicate (1) (Includes Map Transfer-In)	r_M	18	—	56	Ω
Detector (Active and Reference) (1)	r_{DS}, r_{DR}	950	—	2000	Ω
Detector Active/Reference Ratio	—	0.985	—	1.015	—
X Coil Inductance	L_x	34	—	37	μH
Y Coil Inductance	L_y	27	—	30	μH
Z Coil Inductance	L_z	25	—	35	μH
X Coil dc Resistance Non-operating, 25°C	r_x dc	—	2.7	—	Ω
Y Coil dc Resistance Non-operating, 25°C	r_y dc	—	1.1	—	Ω
Z Coil dc Resistance Non-operating, 25°C	r_z dc	—	0.75	—	Ω
X Coil ac Resistance (1)	r_x ac	2.5	—	4.0	Ω
Y Coil ac Resistance (1)	r_y ac	1.5	—	2.5	Ω

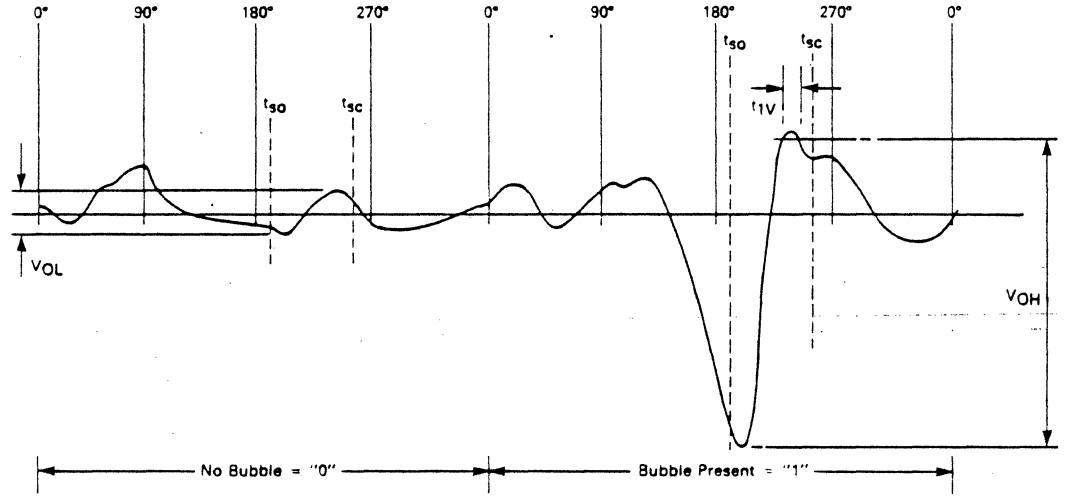
NOTE:
(1) Minimum value is at T_C = 0°C, device non-operating, maximum value is at T_C = 70°C, device operating.

OUTPUT SIGNALS (T_C = 0°C to 70°C, f_o = 125 kHz)

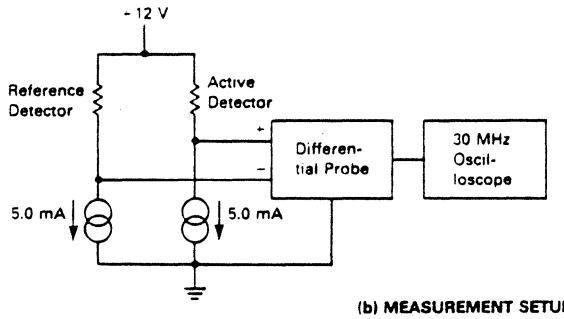
Parameter	Symbol	Min	Typ	Max	Unit
Common-Mode Output Signal (I_{DA} = I_{DR} = 5.0 mA) Differential Peak-to-Peak Output Voltage (1) (I_d = 5.0 mA. See Figure 1 for measurement details.)	V_{cm}	—	—	50	mV
Logic 1 (Bubble Present)	V_{OH}	TBD	—	—	mV
Logic 0 (No Bubble)	V_{OL}	—	—	TBD	mV
Signal Strobe Leading Edge Phase	t_{so}	—	191	—	Degrees
Signal Strobe Trailing Edge Phase	t_{sc}	—	258	—	Degrees
Logic 1 Valid Window	t_{1V}	50	—	—	ns

NOTE:
(1) V_{OH} is defined as the difference between the most negative and the most positive signal excursions which occur within the phase window t_{so} to t_{sc} when a bubble is being detected. V_{OL} is similarly defined for the case of no bubble being detected. See Figure 3.

FIGURE 3 —



(a) DETECTOR BRIDGE OUTPUT



Scope Input Impedance:
≥ 2M
≤ 5.0 pF

Common-Mode Rejection:
≥ 60 dB

Frequency Response:
≥ 5.0 MHz

(b) MEASUREMENT SETUP

Map Read Operation

To read the contents of the map, a series of alternate cycle replicate pulses, identical to data replicate pulses, is applied to pins 10 and 11. Data will be available after t_{PMRD}. Since map data is only loaded into alternate positions in the loop, one pass may result in no data. This procedure is then repeated after delaying one cycle. The outputs from the two map loops are merged, but only one loop contains data. See "Coding of Redundancy Map Loops" for decoding information.

Map Write Operation

Writing the map loop is accomplished by generati map information as normal data on alternate cycle After t_{PGT1} or t_{PGT2}, pins 10 and 11 are pulsed wi a series of negative map transfer pulses on alterna cycles. Selecting t_{PGT1} writes into map loop 1, selecti t_{PGT2} writes into map loop 2.

TIMING CHARACTERISTICS (T_C = 0°C, f_O = 125 kHz unless otherwise noted. See Figure 4 for test conditions).*

WRITE CYCLE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Generate First Bit to Swap In (1)	$t_{PGS(F)}$	—	294	—	Cycles
Generate Last Bit to Swap In (1)	$t_{PGS(L)}$	—	13	—	Cycles
Swap In to Replicate Out (1)	t_{PSR}	—	514	—	Cycles
Swap In to Non-Volatile Storage (2)	t_{PS}	—	2	—	Cycles
Generate Delay Time (3)	t_{DG}	70	—	120	Degrees
Generate Pulse Width (4)	t_{WG}	140	210	280	ns
Generate Fall Time (10%–90% of pk Amplitude)	t_{FG}	200	—	400	ns
Swap Delay Time (3)	t_{DS}	270	—	330	Degrees
Swap Pulse Width	t_{WS}	340	370	400	Degrees

READ CYCLE TIMING

Replicate Out to Detect First Bit (1)	$t_{PRD(F)}$	—	180	—	Cycles
Replicate Out to Detect Last Bit (1)	$t_{PRD(L)}$	—	461	—	Cycles
Replicate Out to Swap In (1)	t_{PRS}	—	510	—	Cycles
Replicate Delay Time (3)	t_{DR}	- 10	—	20	Degree
Replicate Cut Pulse Width	t_{WRC}	210	280	350	ns
Replicate Transfer Pulse Width	t_{WRT}	80	100	120	Degree

MAP READ AND WRITE CYCLE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Map Replicate to Detect	t_{PMRD}	—	188	—	Cycle
Generate to Map Loop #1 Transfer	T_{PGT1}	—	308	—	Cycle
Generate to Map Loop #2 Transfer	t_{PGT2}	—	305	—	Cycles
Map Loop Transfer-In to Replicate	t_{PTR}	—	516	—	Cycles
Map Replicate Delay Time (3)	t_{DRM}	- 10	—	20	Degree
Map Replicate Cut Pulse Width	t_{WRCM}	210	280	350	ns
Map Replicate Transfer Pulse Width	t_{WRTM}	80	100	120	Degree
Map Transfer-In Delay Time	t_{DTM}	270	—	330	Degree
Map Transfer-In Pulse Width	t_{WTM}	200	220	240	Degree

NOTES:

* All pulses to have rise and fall times ≤ 80 ns (10%–90% of peak amplitude) unless otherwise noted.

(1) Propagation times are defined from the beginning of the cycle in which the first signal occurs to the beginning of the cycle in which the seco signal occurs.

(2) Data is non-volatile at the end of the cycle in which the swap current is turned off.

(3) These parameter limits are guaranteed when the device is driven with the X and Y current shown in Figure 4. Deviations from these drive conditions may cause these limits to change in absolute angle, but the phase range (max–min) will remain as specified.

(4) Generate pulse width is defined from 50% amplitude on the rising edge to 90% amplitude on the falling edge.

FIGURE 4 — TEST CONDITIONS — X AND Y CURRENT WAVEFORMS

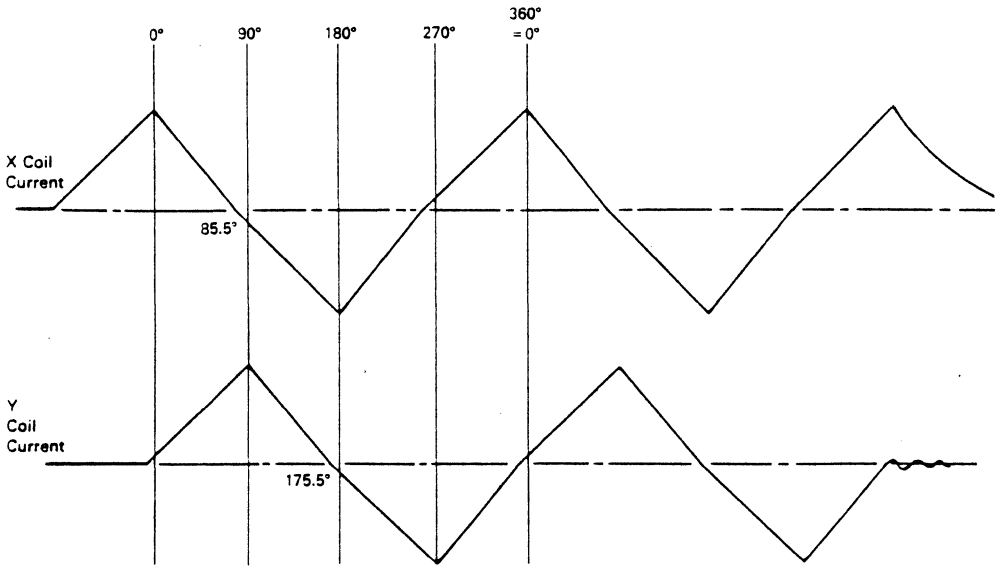
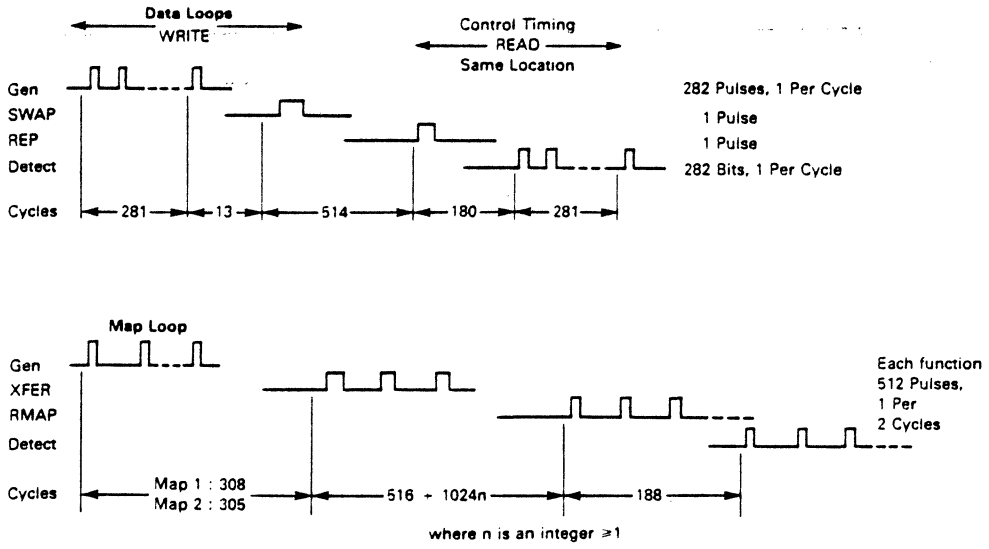


FIGURE 5



Map Read Operation

To read the contents of the map, a series of alternate cycle replicate pulses, identical to data replicate pulses, is applied to pins 10 and 11. Data will be available after t_{PMRD}. Since map data is only loaded into alternate positions in the loop, one pass may result in no data. This procedure is then repeated after delaying one cycle. The outputs from the two map loops are merged, but only one loop contains data. See "Coding of Redundancy Map Loops" for decoding information.

Map Write Operation

Writing the map loop is accomplished by generating map information as normal data on alternate cycles. After t_{PGT1} or t_{PGT2}, pins 10 and 11 are pulsed with a series of negative map transfer pulses on alternate cycles. Selecting t_{PGT1} writes into map loop 1, selecting t_{PGT2} writes into map loop 2.

TIMING CHARACTERISTICS (T_C = 0°C, f_O = 125 kHz unless otherwise noted. See Figure 4 for test conditions).*

WRITE CYCLE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Generate First Bit to Swap In (1)	$t_{PGS(F)}$	—	294	—	Cycles
Generate Last Bit to Swap In (1)	$t_{PGS(L)}$	—	13	—	Cycles
Swap In to Replicate Out (1)	t_{PSR}	—	514	—	Cycles
Swap In to Non-Volatile Storage (2)	t_{PS}	—	2	—	Cycles
Generate Delay Time (3)	t_{DG}	70	—	120	Degrees
Generate Pulse Width (4)	t_{WG}	140	210	280	ns
Generate Fall Time (10%–90% of pk Amplitude)	t_{FG}	200	—	400	ns
Swap Delay Time (3)	t_{DS}	270	—	330	Degrees
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READ CYCLE TIMING

Replicate Out to Detect First Bit (1)	$t_{PRD(F)}$	—	180	—	Cycles
Replicate Out to Detect Last Bit (1)	$t_{PRD(L)}$	—	461	—	Cycles
Replicate Out to Swap In (1)	t_{PRS}	—	510	—	Cycles
Replicate Delay Time (3)	t_{DR}	−10	—	20	Degrees
Replicate Cut Pulse Width	t_{WRC}	210	280	350	ns
Replicate Transfer Pulse Width	t_{WRT}	80	100	120	Degrees

MAP READ AND WRITE CYCLE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Map Replicate to Detect	t_{PMRD}	—	188	—	Cycles
Generate to Map Loop #1 Transfer	T_{PGT1}	—	308	—	Cycles
Generate to Map Loop #2 Transfer	t_{PGT2}	—	305	—	Cycles
Map Loop Transfer-In to Replicate	t_{PTR}	—	516	—	Cycles
Map Replicate Delay Time (3)	t_{DRM}	−10	—	20	Degrees
Map Replicate Cut Pulse Width	t_{WRCM}	210	280	350	ns
Map Replicate Transfer Pulse Width	t_{WRTM}	80	100	120	Degrees
Map Transfer-In Delay Time	t_{DTM}	270	—	330	Degrees
Map Transfer-In Pulse Width	t_{WTM}	200	220	240	Degrees

NOTES:

* All pulses to have rise and fall times ≤ 80 ns (10%–90% of peak amplitude) unless otherwise noted.

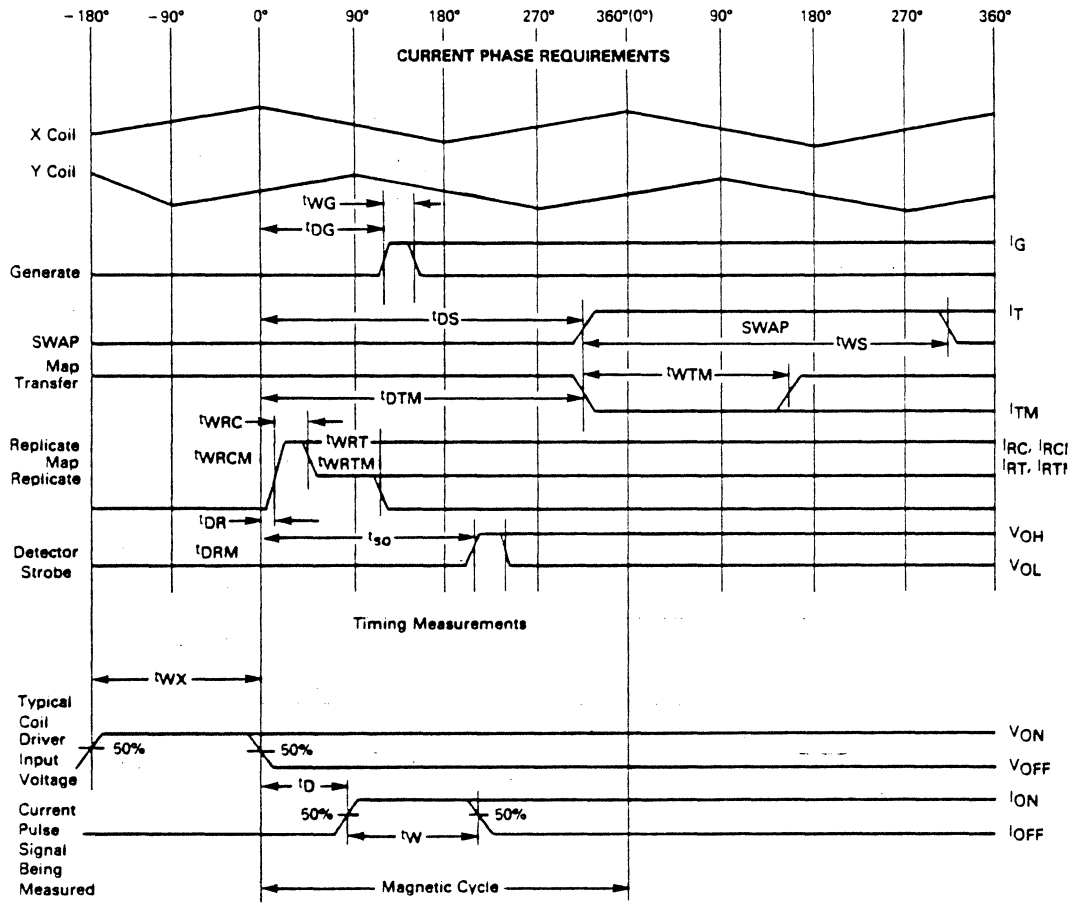
(1) Propagation times are defined from the beginning of the cycle in which the first signal occurs to the beginning of the cycle in which the second signal occurs.

(2) Data is non-volatile at the end of the cycle in which the swap current is turned off.

(3) These parameter limits are guaranteed when the device is driven with the X and Y current shown in Figure 4. Deviations from these drive conditions may cause these limits to change in absolute angle, but the phase range (max–min) will remain as specified.

(4) Generate pulse width is defined from 50% amplitude on the rising edge to 90% amplitude on the falling edge.

FIGURE 6 — X, Y COIL TIMING



TIMING OF PULSES WITHIN A CYCLE

MECHANICAL SPECIFICATION

Package

The MBM2256 device is a 16-pin dual-in-line package. The die is mounted on a printed circuit board carrier attached to a beryllium copper leadframe and encapsulated in plastic compound. Two orthogonal coils and a pair of permanent magnets enclose the die and the whole device is molded into a Mumetal shield. A Z coil is included in the device to facilitate testing and extended temperature range operation.

Mechanical Data

Package Size	1.15 x 1.10 x 0.36 in (29.2 x 27.9 x 9.14) mm
Package Weight	28 gm.

ENVIRONMENTAL SPECIFICATION

Temperature Ranges

Continuous operation at 125 kHz. Case temperature 0° to 70°C. Non-operating, non-volatile storage −40° to 100°C.

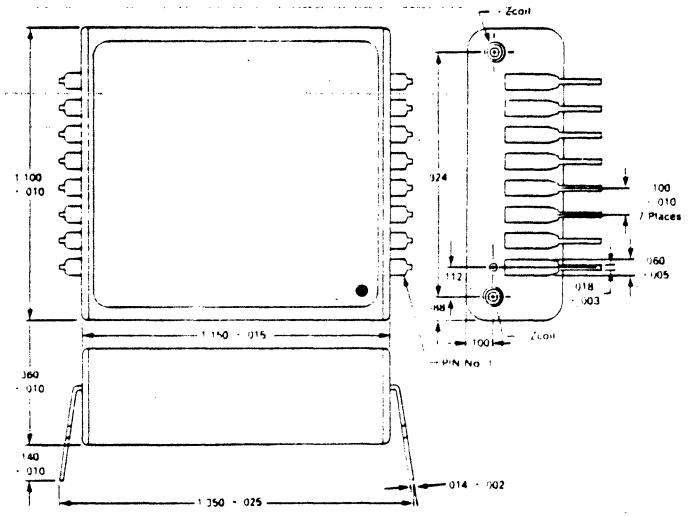
External Magnetic Fields

When subjected to an external magnetic field of 20 Oe maximum in any direction, the device will continue to operate satisfactorily as long as the parameters are kept within the range specified in this document.

Screen Tests	All Parts 100%
Die Visual	100X Inspection consistent with MIL-883B, Method 2010, Cond. B
Stabilization Bake	As per MIL-STD-883B, Method 1008, Condition C, 150°C for 24 hours
Temperature Cycling	As per MIL-STD-883B, Method 1010, Condition B, 10 cycles −55°C → 125°C
External Visual	MIL-883B, Method 2009

Qualification Testing

Bond Strength	MIL-883B, Method 2011.3, Condition D
Mechanical Shock	MIL-883B, Method 2002, Condition B: 1,500G for 0.5 ms
Variable Frequency	MIL-883, Method 2007, Condition A: 20-2,000 Hz for 4 mins.; peak at 20 G's.
Thermal Shock	MIL-883, Method 1011.3, Condition B: −55°C to 125°C, 15 cycles
Moisture Resistance	MIL-883B, Method D 1004.3
Resistance to Solvent	MIL-883B, Method 2015.1
Solderability	MIL-883B, Method 2003.2
Lead Integrity	MIL-883B, Method 2004.3
Flammability	Needle Flame, IEC 695-2-2



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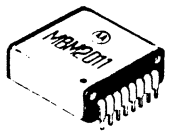
BUBBLE MEMORY PRODUCTS

7402 SOUTH PRICE ROAD • TEMPE, AZ 85283

MBM2011A

Advance Information

1M X 1 BIT MAGNETIC BUBBLE MEMORY DEVICE



GENERAL DESCRIPTION

The MBM2011A is a 1,048,576 (2^{20}) bit magnetic bubble memory device. All required magnetic components, including permanent magnets, the drive field coils and protective magnetic shield are integral parts of the device. The package is a 1.15 x 1.10 x 0.36 inch 16-pin DIP.

The architecture of the MBM2011A features a double-period block-replicate organization with swap gates on the input track. Data storage is organized as 512 storage loops of 2,048 bits each. Additional loops are provided to store the error correction code and as redundant loops. In one of two dedicated map loops on-chip the redundant map loop data is stored.

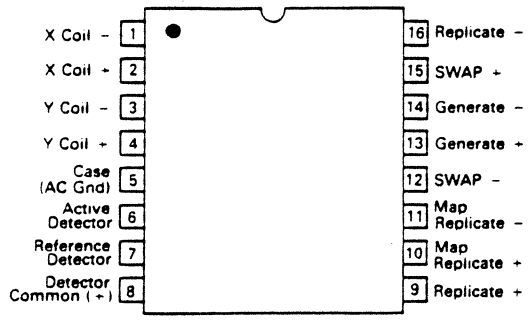
The MBM2011A magnetic bubble memory can be operated synchronously or asynchronously. Average access time to a page of data is less than 11.5 ms at 100 kHz. Data transfer rate is 100 kilobits per second at 100 kHz. Average power dissipation at 100 kHz is 1.0 W. The device will operate over a case temperature range of 0°C to 70°C, and data is retained without power from −40°C to 100°C.

The device is fabricated using a pseudo-planar process to improve operating margins as well as to enhance reliability. The use of CrCuCr in the conductor elements insures excellent conductivity while greatly increasing resistance to problems associated with electromigration.

FEATURES

- Non-volatile
- High Density
- Solid State
- Low Power
- Start/Stop Capability
- Page-Oriented Access
- On-Chip Redundant Loop Map
- Swap Gates
- Block Replicate
- Error Correction Code Storage
- 16-pin Dual-in-Line Package

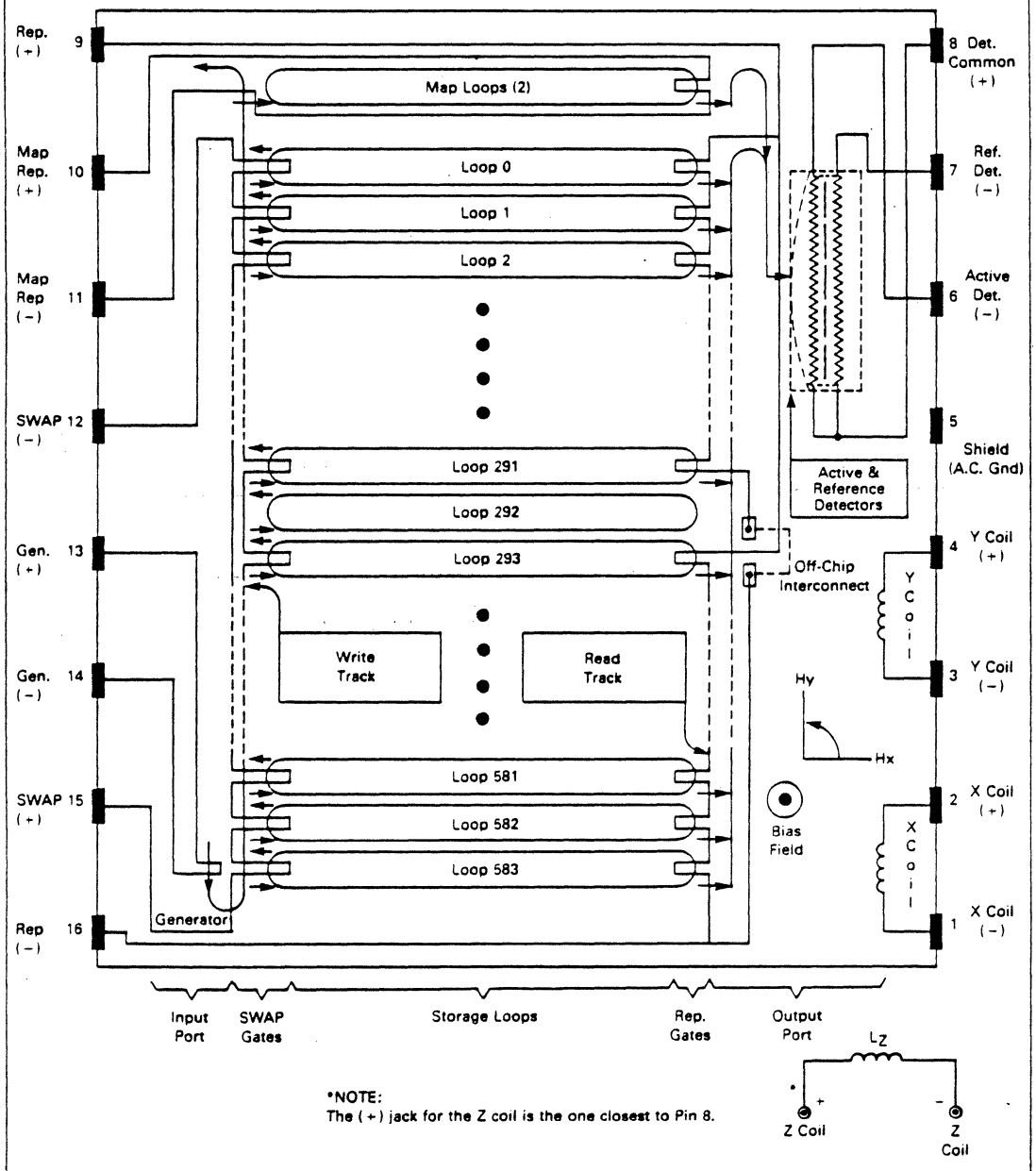
PIN ASSIGNMENTS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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FIGURE 1 — BLOCK DIAGRAM



*NOTE:
The (+) jack for the Z coil is the one closest to Pin 8.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Min	Max	Units
Operating Temperature (Case) (T_C)	0	70	°C
Non-Volatile Storage Temperature	-40	100	°C
Storage Temperature	-40	120	°C
External Magnetic Field	—	20	Oe
Peak Current in X Coil*	—	900	mA
Peak Current in Y Coil*	—	1,100	mA
Peak Current in Z Coil*	—	3,000	mAdc
Peak Replicate Current	—	25	mAdc
Peak Generate Current	—	35	mAdc
Peak Swap Current	—	15	mAdc
Peak Detector Current	—	5.0	mAdc
Coil Disturb Current with Data Retention	—	10	mAdc
Interelement Voltage	—	55	V

*These peak currents are allowed subject to the device temperature not exceeding the temperature limits.

ELECTRICAL CHARACTERISTICS (T_C = 0°C, rotating field frequency (f_o) = 100 kHz)

FUNCTION CURRENTS

Characteristics	Symbol	Min	Typ	Max	Units
Generate Current	I_G	190	—	230	mA
Swap Current	I_S	16	—	20	mA
Data Replicate Cut Current at T_C = 25°C (Note 1)	$I_{RC(25)}$	134	144	154	mA
Data Replicate Transfer Current	I_{RT}	30	—	40	mA
Map Replicate Cut Current at T_C = 25°C (Note 1)	$I_{RCM(25)}$	67	72	77	mA
Map Replicate Transfer Current	I_{RTM}	16	—	20	mA
Map Transfer In Current	I_{TM}	-16	—	-20	mA
Detector Current	I_{DA}, I_{DR}	3.8	4.0	4.2	mA
Temperature Coefficient of Cut Current (Map and Data) Referenced to Value at T_C = 25°C (Note 1)	α_{RC}	-0.32	-0.34	-0.36	%/°C

Note 1: Map and Data replicate cut currents require temperature compensation. The current at any case temperature, T_C, is given by:

$$I_{RC(T)} = I_{RC(25)}\left[1 + \frac{\alpha_{RC}}{100}(T-25)\right] \quad 0 \le T \le 70°C \qquad I_{RCM(T)} = I_{RCM(25)}\left[1 + \frac{\alpha_{RC}}{100}(T-25)\right] \quad 0 \le T \le 70°C$$

COIL DRIVES (See Figure 2)

Characteristics	Symbol	Min	Typ	Max	Units
Coil Driver Supply Voltage	V_x, V_y	11.4	12	12.6	V
Coil Driver Switch on Resistance (2 switches in series)	R_{on}	0.7	—	1.8	Ω
Coil Driver Clamp Diode Drop (2 diodes in series)	V_{clamp}	—	—	1.6	V
X Coil Peak Current (L_x = nom, V_x = nom) (R_{on}, V_{clamp} = nom)	I_{XP}	—	650	—	mA
Y Coil Peak Current (L_y = nom, V_y = nom) (R_{on}, V_{clamp} = nom)	I_{YP}	—	740		mA
Coil Current Offset	I_{xo}, I_{yo}	-10	—	10	mA
Stop Current Overshoot	I_{so}	—	—	+10 -0	mA
Total Coil Power	P_c	—	—	1.4	W
Z-Coil Sensitivity		—	26.5	—	Oe/A
Z-Coil Current to Simultaneously Erase All Data Stored Rotating Field On Rotating Field Off	I_{zap}	2.0 3.0	— —	— —	A
Duration of Erase Current	t_{ZAP}	0.5	—	10	ms

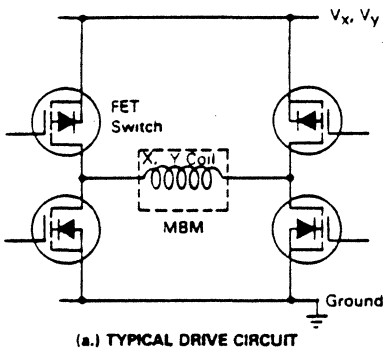
SCOPE

This specification describes the magnetic, electrical, mechanical and environmental parameters of the 1Mbit magnetic bubble device, MBM2011A as manufactured by Motorola Inc.

DEVICE ORGANIZATION

The 1Mbit bubble memory chip uses a block-replicate organization with swap gates on the input track. The storage area is arranged as 512 storage loops each, with 2,048 bit locations. Additional loops are provided for error correction (12), and defect tolerance (60), giving a total of 584 loops. Data is written and read at the clock frequency which is the rotating field frequency. Figure 1 is a schematic diagram of the 1Mbit chip.

FIGURE 2 — X, Y COIL DRIVE



(a.) TYPICAL DRIVE CIRCUIT

Data Input

To write into the device, the single generator is pulsed and the data pattern is propagated along the double period input track until it aligns with the storage loops. Operating the swap gates transfers the new data into the storage loops such that consecutive bits go into adjacent loops and simultaneously transfer out the old data.

Data Output

To read data, the replicate gate is pulsed and one bit is replicated from each loop into the double period output track. The data then propagates along the output track and through the detector such that data is read out at the clock frequency.

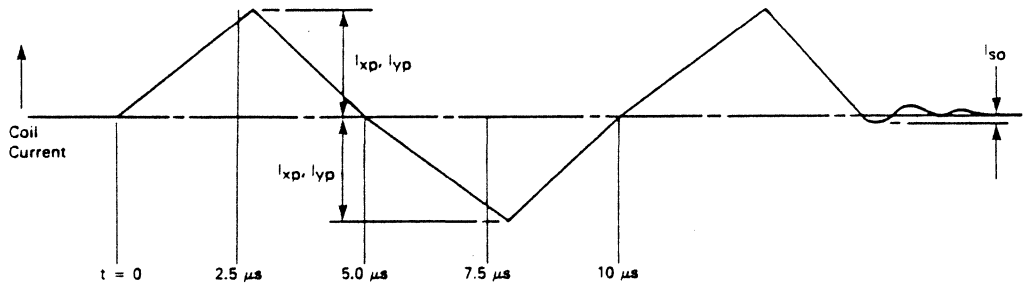
Redundancy

Of the 584 storage loops, 512 are allocated for data, 12 for error correction and 60 for redundancy. These 60 loops are used to mask inoperable minor loops and improve performance. Sixty loops are always declared redundant. Data should not be written into the redundant loops.

Redundancy Map

In addition to the 584 storage loops, the chip contains two map loops. These loops have their own transfer-in and replicate gates but share the generator and detector with the storage loops. Only one loop is required and is chosen at final test. The chosen loop is used to store the data which identifies the redundant loop map. A 'one' designates a usable loop; a 'zero,' a non-usable loop. Preceding this map code is a stream of 64 'zeros' followed by a 'one' and a 'zero' which may be used to synchronize the external control circuitry with the memory. The map loop used for storage of the redundancy information is also identified in the code (see "Coding of Redundancy Map"). Since only alternate bit positions are written into the map loop to enhance reliability, intervening bits are always zero and are ignored during read (see "Map Read Operation").

The redundancy map is also printed on the label of each device using hexadecimal format. Two digits are used per loop. Instead of providing the absolute loop number, the incremental difference between non-usable loops is printed. For example, if the first bad loop is #7, and the next two are 19 and 23, the sequence 070C04 will be printed on the label. This format allows for an incremental difference between two non-usable loops of up to 255 (FF). Loop #292 is not connected in the 1Mbit device and is always declared bad.



(b.) TYPICAL RISE/FALL IMBALANCE DUE TO DRIVE CIRCUIT

Coding of Redundancy Map. The map loop contains 1024 bits of information in five fields.

Pattern	Field	Number of Bits	Notes
MM....MM	Map Data	584	(1)
EE...EE	Error Correction	12	(2)
LL	Loop	2	(3)
UU...UU	User	360	(4)
00....0010	Sync	66	(5)

(1) Each bit corresponds to a data loop in sequence
M = 1 identifies a usable loop (524).
M = 0 identifies a redundant loop (60).
(2) Error correction code used is a fire code applied only to the map data.
(3) Identifies which map loop contains the redundancy information 01 — loop #1, 10 — loop #2.
(4) This field may contain factory-pertinent information. It will not contain a duplicateof the sync pattern.
(5) The sync pattern is used to locate the beginning of the map data field and identifies data page zero.

Organizational Specifications

Bits/Loop	2,048
Total Data Loops	584
Usable Data Loops	524
Error Correction Loops	12
User Data Loops	512
Total User Storage	1,048,576 bits
Map Loops	2

FUNCTIONAL DESCRIPTION

Write Data Operation

Writing data is accomplished by generating a pattern with a series of pulses applied to pins 13 and 14, starting t_{PGSF} before the swap operation. As the device continues to cycle after all data is generated, the new data and the old will be aligned at the swap gates after t_{PGSL}. A swap pulse is applied to pins 12 and 15 at this time, swapping the new data in and the old data out. The old data are propagated out and discarded beyond the active area.

Note: In order to ensure correct device operation, it is essential that at least one empty bit position follows the last bit of a data block.

Read Data Operation

To read data, the device must be cycled until the desired page is aligned with the replicate gates on the output side of the storage loops. A replicate cut pulse is applied to pins 9 and 16 to duplicate the page. This is immediately followed by a replicate transfer pulse which causes the duplicate bubbles to propagate into the output track.

Detection occurs when a bubble passes under the magnetoresistive detector element. The bubble's magnetic field causes the detector element to change resistance. By passing a constant current through the detector, this is converted to a voltage signal. A dummy detector which is not influenced by magnetic bubbles is used to cancel the background magnetoresistive signal.

Output bubbles are discarded beyond the active area after detection. A complete page is read in t_{PRDL}.

INTERFACE IMPEDANCES

Characteristics	Symbol	Min	Typ	Max	Units
Generate (2)	r_G	4.0	—	11	Ω
Swap (2)	r_S	500	—	1150	Ω
Replicate (2)	r_R	90	—	160	Ω
Map Replicate (Includes Map Transfer-In) (2)	r_M	28	—	65	Ω
Detector (Active and Reference) (2)	R_{DA}, r_{DR}	900	—	2000	Ω
Detector Active/Reference Ratio		0.985	—	1.015	
X Coil Inductance	L_x	41	—	44	μH
Y Coil Inductance	L_y	36	—	39	μH
Z Coil Inductance	L_z	25	—	35	μH
X Coil dc Resistance Non-Operating, 25°C	r_x	—	3.3	—	Ω
Y Coil dc Resistance Non-Operating, 25°C	r_y	—	1.5	—	Ω
Z Coil dc Resistance Non-Operating, 25°C	r_z	—	0.75	—	Ω
X Coil ac Resistance (2)	r_x	3.3	—	5.3	Ω
Y Coil ac Resistance (2)	r_y	2.1	—	3.1	Ω

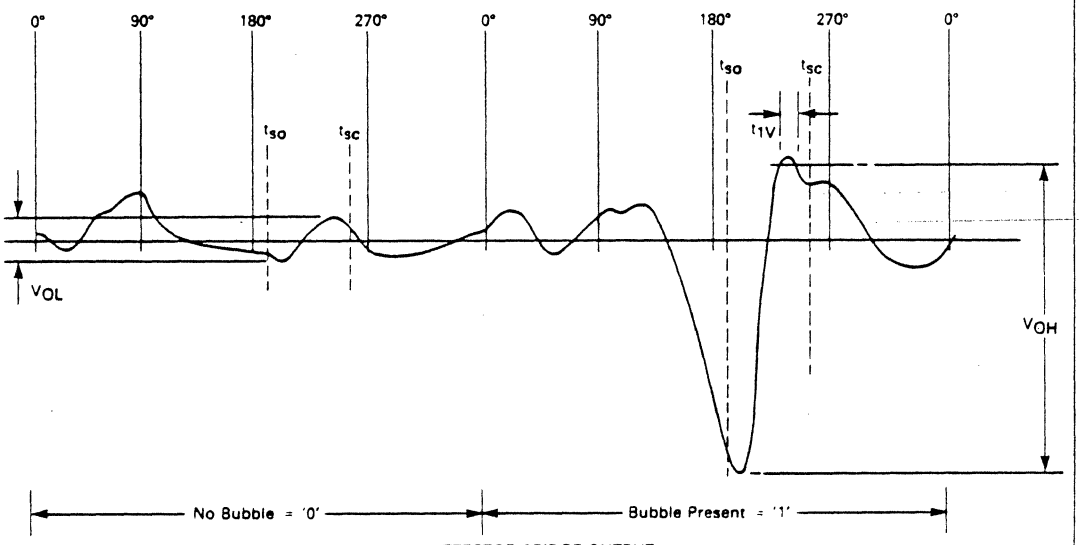
NOTE:
(2) $T_{C(min)}$ = 0°C, non-operating
$T_{C(max)}$ = 70° C, operating

OUTPUT SIGNALS (T_C = 0°C to 70°C, f_O = 100 kHz)

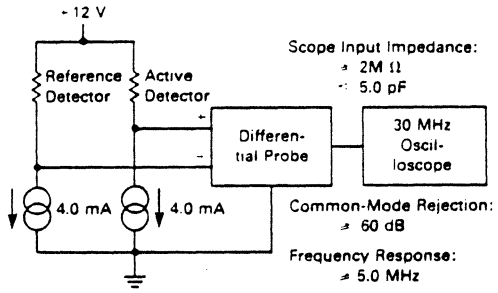
Characteristic	Symbol	Min	Typ	Max	Units
Common-Mode Output Signal (I_{DA} = I_{DR} = 4.0 mA) Differential Peak-to-Peak Output Voltage (See Note 1) I_d = 4.0 mA, See Figure 1 for measurement details)	V_{cm}	—	—	50	mV
Logic 1 Bubble Present	V_{OH}	TBD	—	—	mV
Logic 0 No Bubble	V_{OL}	—	—	TBD	mV
Signal Strobe Leading Edge Phase	t_{so}		191		Degrees
Signal Strobe Trailing Edge Phase	t_{sc}		258		Degrees
Logic 1 Valid Window	t_{1V}	50			ns

Note 1: V_{OH} is defined as the difference between the most negative and the most positive signal excursions which occur within the phase window t_{so} to t_{sc} when a bubble is being detected. V_{OL} is similarly defined for the case of no bubble being detected. See Figure 3.

FIGURE 3



(a) DETECTOR BRIDGE OUTPUT



(b) MEASUREMENT SETUP

Map Read Operation

To read the contents of the map, a series of alternate cycle map replicate pulses is applied to pins 10 and 11. Data will be available after t_{PMRD}. Since map data is only loaded into alternate positions in the loop, one pass may result in no data. In this case, the procedure is repeated after delaying one cycle. The outputs from the two map loops are merged, but only one loop contains data. See "Coding of Redundancy Map Loops" for decoding information.

Map Write Operation

Writing the map loop is accomplished by generating map information as normal data on alternate cycles. After t_{PGT1} or t_{PGT2}, pins 10 and 11 are pulsed with a series of negative map transfer pulses on alternate cycles. Selecting t_{PGT1} writes into map loop 1, selecting t_{PGT2} writes into map loop 2.

TIMING CHARACTERISTICS T_C = 0°C to 70°C, f_O = 100 kHz. See Figure 4 for test conditions. All control pulses to have rise and fall times ≤ 80 ns (10%–90% of pk amplitude) unless otherwise noted. All pulsewidths measured at 50% amplitude unless otherwise noted.

WRITE CYCLE TIMING

Characteristic	Symbol	Min	Typ	Max	Units
Generate First Bit to Swap In (1)	$t_{PGS(F)}$	—	597	—	Cycles
Generate Last Bit to Swap In (1)	$T_{PGS(L)}$	—	14	—	Cycles
Swap In to Replicate Out (1)	t_{PSR}	—	1026	—	Cycles
Swap In to Non-Volatile Storage (2)	t_{PS}	—	2	—	Cycles
Generate Delay Time (3)	t_{DG}	70		120	Degrees
Generate Pulse Width (4)	t_{WG}	100	150	200	ns
Generate Fall Time (80%–90% of pk Amplitude)	t_{FG}	200		400	ns
Swap Delay Time (3)	t_{DS}	270		330	Degrees
Swap Pulse Width	t_{WS}	340	370	400	Degrees

READ CYCLE TIMING

Replicate Out to Detect First Bit (1)	$t_{PRD(F)}$	—	91	—	Cycles
Replicate Out to Detect Last Bit (1)	$t_{PRD(L)}$	—	674	—	Cycles
Replicate Out to Swap In (1)	t_{PRS}	—	1022	—	Cycles
Replicate Delay Time (3)	t_{DR}	0		12	Degrees
Replicate Cut Pulse Width	t_{WRC}	50	75	100	ns
Replicate Transfer Pulse Width	t_{WRT}	80	100	120	Degrees

MAP READ AND WRITE CYCLE TIMING

Characteristic	Symbol	Min	Typ	Max	Units
Map Replicate to Detect	t_{PMRD}	—	97	—	Cycles
Generate to Map Loop # 1 Transfer	t_{PGT1}	—	608	—	Cycles
Generate to Map Loop #2 Transfer	t_{PGT2}	—	605	—	Cycles
Map Loop Transfer-In to Replicate	t_{PTR}	—	1028	—	Cycles
Map Replicate Delay Time (3)	t_{DRM}	0	—	12	Degrees
Map Replicate Cut Pulse Width	t_{WRCM}	50	75	100	ns
Map Replicate Transfer Pulse Width	t_{WRTM}	80	100	120	Degrees
Map Transfer-In Delay Time	t_{DTM}	270	—	330	Degrees
Map Transfer-In Pulse Width	t_{WTM}	200	220	240	Degrees

NOTES: (1) Propagation times are defined from the beginning of the cycle in which the first signal occurs to the beginning of the cycle in which the second signal occurs.

(2) Data is non-volatile at the end of the cycle in which the swap current is turned off.

(3) These parameter limits are guaranteed when the device is driven with the X and Y current shown in Figure 4. Deviations from these drive conditions may cause these limits to change in absolute angle, but the phase range (max.-min.) will remain as specified.

(4) Generate pulse width is defined from 50% amplitude on the rising edge to 90% amplitude on the falling edge.

FIGURE 4 — TEST CONDITIONS — X AND Y CURRENT WAVEFORMS

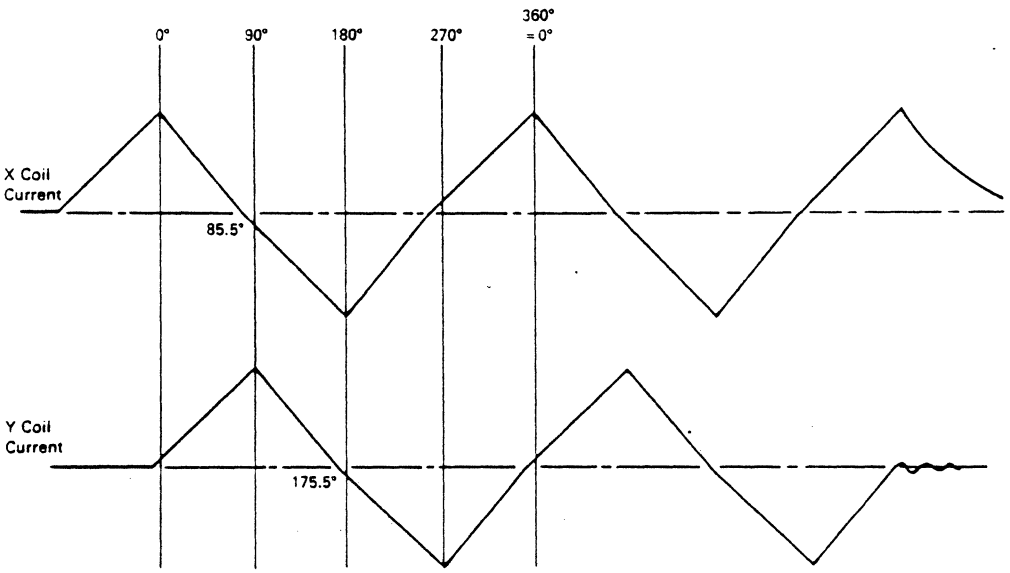
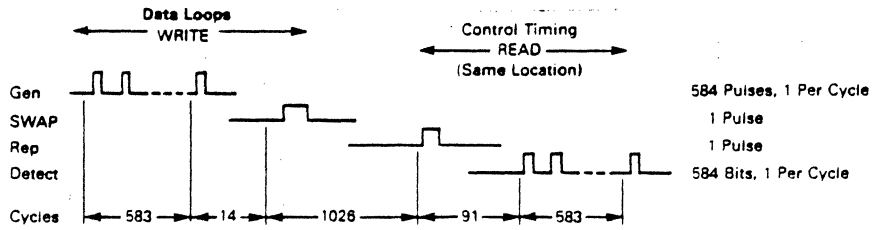


FIGURE 5



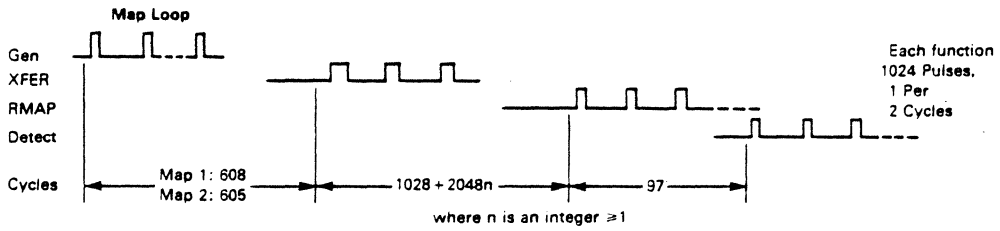
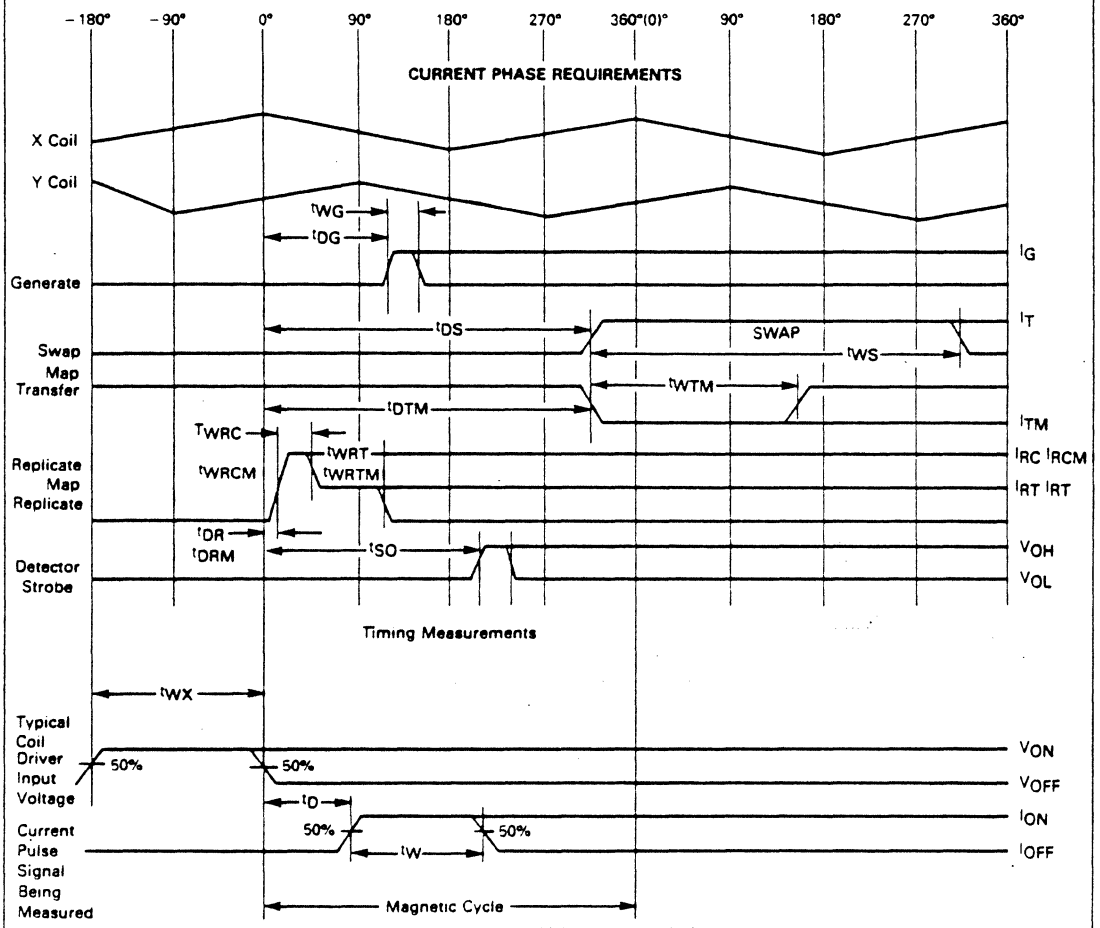


FIGURE 6 — X, Y COIL TIMING



TIMING OF PULSES WITHIN A CYCLE

MECHANICAL SPECIFICATION

Package

The MBM2011A device is a 16-pin dual-in-line package. The die is mounted on a printed circuit board carrier attached to a beryllium copper leadframe and encapsulated in plastic compound. Two orthogonal coils and a pair of permanent magnets enclose the die and the whole device is molded into a Mumetal shield. A Z coil is included in the device to facilitate testing and extended temperature range operation.

Mechanical Data

Package Size	1.15 x 1.10 x 0.36 in (29.2 x 27.9 x 9.14) mm
Package Weight	28 gm.

ENVIRONMENTAL SPECIFICATION

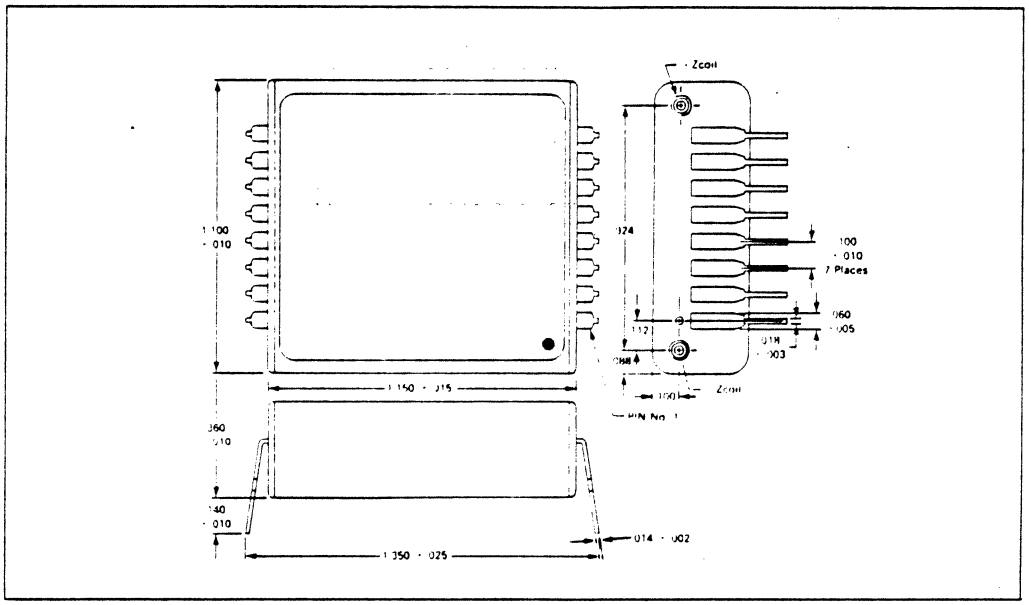
Temperature Ranges
(See "Absolute Maximum Ratings").

External Magnetic Fields
When subjected to an external magnetic field of 20 Oe maximum in any direction the device will continue to operate satisfactorily as long as the parameters are kept within the range specified in this document.

Screen Tests	All Parts 100%
Die Visual	100X Inspection consistent with MIL-883B, Method 2010, Cond. B
Stabilization Bake	As per MIL-STD-883B, Method 1008, Condition C, 150°C for 24 hours
Temperature Cycling	As per MIL-STD-883B, Method 1010, Condition B, 10 cycles −55°C → 125°C
External Visual	MIL-883B, Method 2009

Qualification Testing

Bond Strength	MIL-883B, Method 2011.3, Condition D
Mechanical Shock	MIL-883B, Method 2002, Condition B: 1,500G for 0.5 ms
Variable Frequency	MIL-883, Method 2007, Condition A: 20-2,000 Hz for 4 mins.; peak at 20 G's.
Thermal Shock	MIL-883, Method 1011.3, Condition B: −55°C to 125°C, 15 cycles
Moisture Resistance	MIL-883B, Method D 1004.3
Resistance to Solvent	MIL-883B, Method 2015.1
Solderability	MIL-883B, Method 2003.2
Lead Integrity	MIL-883B, Method 2004.3
Flammability	Needle Flame, IEC 695-2-2



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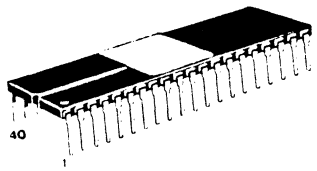
BUBBLE MEMORY PRODUCTS

7402 SOUTH PRICE ROAD • TEMPE, AZ 85283

SC42584
SC42585

Advance Information

BUBBLE MEMORY CONTROLLERS



GENERAL DESCRIPTION

The SC42584 and SC42585 Bubble Memory controllers are monolithic HMOS integrated circuits which control the operation of the Motorola MBM2256 (256 Kilobit) and MBM2011 (1 Megabit) Magnetic Bubble Memories, respectively. They provide the interface between a Magnetic Bubble Memory (MBM) subsystem and the user system, including data and map loop read and write, redundant loop management, error correction, and all bubble memory timing. The SC42584 and SC42585 are functionally equivalent and pin-compatible. They differ only in data record length and bubble memory control pulse timing. They are packaged in 40-pin dual-in-line packages with 0.6-inch pin row spacing.

FEATURES

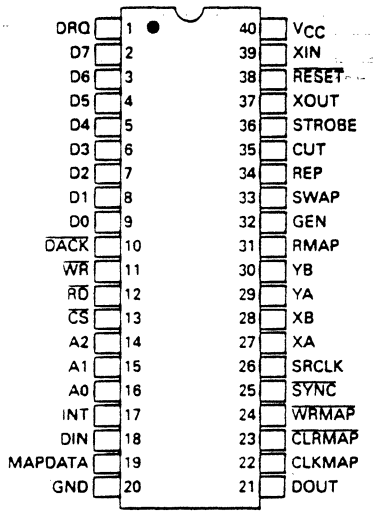
- Single-Chip Integrated Circuit
- Generation of All Bubble Memory Timing Signals
- Operation of 1 to 8 Bubble Memories in Parallel
- Complete Error Correction/Detection
- Dynamic Data Buffering of 16 Bytes
- Complete Redundant Loop Management
- Direct 8-bit Microprocessor Bus Interface
- Programmed, Interrupt, or DMA Data Transfer
- Power-Failure Interlock
- On-chip Crystal-Controlled Oscillator
- Simple Software Interface with Diagnostic Capability
- Bootloop Write with Mechanical Interlock

ABSOLUTE MAXIMUM RATINGS*

Characteristics	Value	Unit
Ambient temperature with power applied		
Commercial device	0 to + 70	°C
Extended-temperature device	−55 to + 125	°C
Storage Temperature	−65 to + 150	°C
Voltage — any pin with respect to GND	−0.5 to + 7.0	Volts
Power dissipation	1.0	Watts

* Absolute Maximum Ratings indicate limits beyond which permanent damage may occur to the device. Proper operation of the device requires that it be limited to the conditions specified under DC Electrical Characteristics.

FIGURE 1 — PIN ASSIGNMENTS



40-pin dual in-line package;
0.6-inch row spacing

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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PIN DESCRIPTIONS

User Interface

$\overline{\text{RESET}}$ — If a command is executing, initiates an orderly termination; resets and preconditions internal registers and control logic.

Data Bus (D7–D0) — Bidirectional transfer of data, commands, and status between the user system and the controller.

Address (A2–A0) — Selects one of eight internal registers for bus transfer.

$\overline{\text{CS}}$ — Chip Select — enables the user data-bus interface.

$\overline{\text{RD}}$ — Read Enable — enables reading from the addressed register in conjunction with $\overline{\text{CS}}$ or $\overline{\text{DACK}}$.

$\overline{\text{WR}}$ — Write Enable — enables writing to the addressed register in conjunction with $\overline{\text{CS}}$ or $\overline{\text{DACK}}$.

INT — Interrupt — programmable to indicate data request or command completion.

DRQ — Data Request — indicates that the controller is ready for a data byte transfer to or from the user system.

$\overline{\text{DACK}}$ — Data Acknowledge — enables a transfer between the bus and the data buffer in conjunction with $\overline{\text{RD}}$ and $\overline{\text{WR}}$ but independent of A2–A0. .

External Map Memory Interface

MAPDATA — Data from external redundancy-map memory.

$\overline{\text{CLRMAP}}$ — Initializes (clears to zero) the redundancy-map memory address counter.

CLKMAP — Rising edge increments the redundancy-map memory address counter.

$\overline{\text{WRMAP}}$ — Enables writing data from the MBM(s) to the redundancy-map memory.

Supplies and Miscellaneous

XIN, XOUT — Crystal connections for controller clock oscillator. Alternatively, XIN may be driven with an externally-generated square wave at standard TTL levels, in which case, XOUT should be left unconnected.

V_{CC} — Power supply voltage: 5 V ± 5 percent.

GND — System ground.

Bubble Memory Interface

DIN — Data In — serial data from MBM sense amplifier (single-MBM bank) or parallel-to-serial shift register (multiple-MBM bank).

DOUT — Data Out — serial data to MBM operation driver (single-MBM bank) or to serial-to-parallel shift register (multiple-MBM bank).

STROBE — Data timing signal — defines sample window for sense amplifier. Trailing edge latches detected data in sense amplifier. Leading edge latches data into operation driver in single-MBM bank.

$\overline{\text{SYNC}}$ — Data timing for multiple-MBM bank. Loads data from sense amplifiers into a parallel-to-serial shift register. Trailing (rising) edge clocks data from a serial-to-parallel shift register into the operation driver(s).

SRCLK — Clock for shift registers used in a multiple-MBM bank. Rising edge advances shift registers. Falling edge internally samples data on DIN or changes data on DOUT.

GEN — Generate
SWAP — Swap
REP — Replicate
RMAP — Replicate Map
CUT — Cut

Timing signals to operation driver which control the corresponding currents. Cut current is produced by the conjunction of CUT and REP or CUT and RMAP.

XA — X coil positive current enable.
XB — X coil negative current enable.
YA — Y coil positive current enable.
YB — Y coil negative current enable.

When the –A and –B signals are both high, the corresponding coil is off and both ends are grounded.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Volts ±5% unless otherwise specified.)

Parameter	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	-0.5	0.8	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −500 μA)	V_{OH}	2.4	—	V
V_{OH} for XA,XB,YA,YB (1)	V_{COH}	2.4	—	V
XIN Input Low Voltage	V_{XINL}	-0.5	0.4	V
XIN Input High Voltage	V_{XINH}	2.4	V_{CC} + 0.5	V
Input Current (V_{IN} = 0 to V_{CC})	I_{IL}	—	10	μA
Output Off-state Current (V_{OUT} = .45 to V_{CC})	I_{OZ}	-10	10	μA
V_{CC} Supply Current (V_{CC} = 5.25 V)	I_{CC}	—	150	mA

(Note 1) V_{CC} = 5 V, I_{OH} = − 0.5mA
V_{CC} = 2.8 V, I_{OH} = −0.1mA

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Clock Period	t_{CY}	100	333	ns
Clock High Time	t_{CH}	0.4	0.6	t_{CY}
Clock Rise Time	t_{CR}	—	25	ns
Clock Fall Time	t_{CF}	—	25	ns
$\overline{RESET}$ Pulse Width	t_{WRE}	64	—	t_{CY}
Reset Disable Delay	t_{DRD}	—	192	t_{CY}
DRQ Turn Of Delay	t_{DDR}	—	300	ns
INT Turn Off Delay	t_{DIN}	—	150	ns
$\overline{CS}$ & Address Set Up	t_{AS}	25	—	ns
$\overline{CS}$ & Address Hold	t_{AH}	0	—	ns
Time Between Successive $\overline{RD}$ Pulses	t_{ROFF}	2.0	—	t_{CY}
Read Data Delay (C_L = 30 pF) (C_L = 100 pF)	t_{DDR}	— —	250 300	ns ns
Data Bus Turn Off (C_L = 20 − 100 pF)	t_{DZ}	20	100	ns
$\overline{WR}$ Pulse Width	t_{WW}	200	—	ns
Time Between Successive $\overline{WR}$ Pulses	t_{WOFF}	2.0	—	t_{CY}
Write Data Set Up	t_{DSW}	25	—	ns
Write Data Hold	t_{DHW}	25	—	ns
DIN, MAPDATA Set Up	t_{DIS}	50	—	ns
DIN, MAPDATA Hold	t_{DIH}	50	—	ns
DOUT Delay	t_{DOD}	—	100	ns

BUBBLE MEMORY DEVICE OPERATION

The magnetic bubble memory (MBM) device stores data as the presence or absence of locally-polarized domains referred to as bubbles in a thin film of magnetic garnet material. A pattern of magnetic material on the surface defines stable locations for the bubbles and paths between them. A rotating magnetic field is produced in the plane of the film by two orthogonal coils within the MBM package. One cycle of field rotation advances all bubbles one position on their respective tracks. The field may be stopped at the end of any cycle, and the bubbles will remain in place.

The data storage area is organized as a number of closed storage loops. Input and output tracks carry bubbles to and from the storage loops and are interconnected with the loops at opposite ends by swap and replicate gates respectively. One physical page of data consists of one bit from each of the storage loops. Figure 2 is a functional diagram of the MBM. Actual implementation may be different. Table 1 gives the MBM capacities.

A generator creates bubbles in the input track as required to write data into the MBM. When a number of data bits equal to the number of storage loops has been entered into the input track and shifted into alignment with the loops, a swap pulse is applied which interchanges each bit in the input track with one bit in the adjacent storage loop. The bits swapped out are shifted to the end of the input track and annihilated.

To read data non-destructively, a replicate-cut-transfer pulse is applied. This pulse causes a stretched bubble at the replicate gate of each storage loop to be cut into two full-sized bubbles with the trailing bubble transferred to the output track while the leading bubble remains in the storage loop. Bubbles in the output track are then shifted to the detector which consists of a matched pair of magneto-resistive elements. Bubbles pass beneath the active detector element causing a change in its resistance, and are then destroyed. A constant current passed through the detector converts the resistance change into a voltage change. The reference detector element provides cancellation of noise induced by the rotating field, through the use of differential detection.

In order to improve MBM device yields, extra redundant storage loops are provided, and the device is permitted to have a limited number of non-functioning loops. Since data transfer between the controller and the MBM is bit serial, if the controller knows the locations of the non-functioning loops, it can skip over them. For this purpose, two additional storage loops are provided, one of which is loaded at the factory with a map of the useable data loops; the other is empty. The map loops communicate with the same input and output tracks as the data loops, but have separate control inputs for replicate and transfer-in (the map write function does not perform a true swap).

SYSTEM DESCRIPTION

The Magnetic Bubble Memory Controller provides the complete interface between a user system and a magnetic bubble memory subsystem. The user communicates with the controller via an eight-bit parallel bidirectional data bus which carries commands, data, status, and associated control information. This data bus is designed to connect directly to a microprocessor system. The controller contains eight internal registers which can be mapped via three address lines directly into memory locations or I/O ports in the user system.

The controller is specifically designed to interface with the following Motorola bubble memory devices and support circuits:

- MBM2256 and MBM2011 Magnetic Bubble Memories — 256 kilobit and one megabit devices respectively.
- SC42468 Coil Pre-driver — provides the necessary drive for the X and Y coil drivers (MOS power FETs) and also provides power supply low-voltage detection.
- MC34046 and MC34047 Operation Drivers — provide the generate, swap, replicate, and map replicate current pulses for the MBM2256 and MBM2011 respectively.
- MC34044 Sense Amplifier — provides the detector bias currents and bubble signal detection.

The controller can operate 1, 2, 4, or 8 MBMs in parallel, each with its own support circuits. Parallel operation multiplies the single-MBM physical page size and data transfer rate by the number of MBMs operated (1, 2, 4, or 8). Consecutive data bits are written to and read from adjacent MBM devices cyclically; therefore each data record is distributed across all the MBMs. Single and multiple MBM systems are shown in Figures 3a and 3b.

The controller can be interfaced to several banks of MBMs, each containing multiple MBMs (not necessarily the same number). This is accomplished by using the chip select inputs on the support devices to enable one bank at a time using an externally latched and decoded address. The controller operates the various banks independently, and it must be reinitialized whenever the active bank is changed. A multiple-bank system is shown in Figure 3c.

A multiple-MBM bank requires additional components as follows:

1) an eight-bit serial-to-parallel shift register which receives data from DOUT clocked by SRCLK, and from which data is transferred in parallel to the operation drivers by $\overline{\text{SYNC}}$. Banks of two or four MBMs use the positions corresponding to the first bits shifted in.
2) a parallel-to-serial shift register which receives data from the sense amplifiers enabled by $\overline{\text{SYNC}}$ and shifts the data to DIN clocked by SRCLK. The bit length need be only as great as the number of MBMs.

The controller accepts only the first two or four bits shifted in for corresponding bank sizes.

3) an external redundancy-map memory and address counter (not required for two MBM2256s) to augment the controller's internal map memory. This memory subsystem is connected as shown in Figure 4. It uses the following controller signals which are described under PIN DESCRIPTIONS: $\overline{\text{CLRMAP}}$, CLKMAP, $\overline{\text{WRMAP}}$, and MAPDATA. The memory is configured as one bit wide, and is written and read serially. Map memory timing is shown in Figure 9.

In some applications, the user may wish to have the redundancy map data permanently stored in a PROM. This may be done using the configuration described in 3). In this case, the controller's internal map memory is not used.

CONTROLLER OPERATION

A block diagram of the main functional components of the controller is given in Figure 5.

User Interface

The user interface is directly compatible with many 8-bit microprocessors. The data bus provides user communication with any of the eight internal registers as selected by the address input. The INT signal can be used to interrupt the processor to request data or to indicate command termination. The DRQ and $\overline{\text{DACK}}$ signals can interface to a separate Direct-Memory-Access controller. These functions are described in detail under PROGRAMMING INFORMATION.

Data Path

The DATA BUFFER provides sixteen bytes of dynamic buffering between the user and the bubble memory subsystem. Bytes are transferred in parallel between the buffer and the SHIFTER which performs the serial-to-parallel conversion on data read from the MBM(s) through DIN or the parallel-to-serial conversion on data to be written to the MBM(s) over DOUT.

When writing, the OUTPUT MAPPER inserts zeros into the data stream at positions corresponding to the unused loops. The INPUT MAPPER deletes the corresponding bits from the input stream when reading. The redundant loop map is accessed from the MAP MEMORY during these operations and provided to the mappers. The ERROR CORRECTION circuit generates check bits and inserts them into the data stream when writing, and checks these bits when reading. It is capable of correcting any single burst of errors up to three bits long via the READ CORRECTED command.

The redundancy-map data is usually stored in one of the two separate map loops in the MBM. The controller reads this data during initialization, and stores it in the MAP MEMORY from which it is retrieved during data read and write operations. The controller has on-chip map memory sufficient to store the map for one MBM2011 or two MBM2256s. For multiple-MBM banks, additional external memory is required; the controller provides all the control signals necessary to operate this external memory.

Alternatively, the map data can be permanently stored in an external PROM or a completely external RAM may be used. In either case, the entire map is read from the external memory, and the internal map memory is not used.

The map loop also contains a synchronization pattern which is used to locate sector/page zero during initialization. The map loop is normally loaded at the factory and need only be read to initialize the controller. However, commands are provided to read and write the map loops for diagnostic purposes or to change the map loop contents. Since the map loop write uses a transfer-in rather than a swap function, the MBM must be erased using the Z-coil or an external magnetic field prior to a map write. The map transfer-in pulse is generated on the SWAP pin. A switch is required as shown in Figure 6 to properly route the current pulse to the MBM. This switch also protects against accidental destruction of the map data by an unintentional map write.

Redundant loop data are stored in alternate bit positions in one of the map loops in the MBM. The intervening bit positions and the other map loop must contain all zeros (no bubbles). All map operations access only alternate map bits so the intervening zeros are not seen by the controller. (Initialization may start in the wrong phase and read only the intervening zeros. In this case, it automatically shifts one position and rereads.) Data from the two map loops are merged when reading so that loop selection is not required. The WRITE MAP command allows specification of the desired loop.

The format of the map loop data is shown in Table 3.

Bubble Memory Data and Timing

All the necessary MBM coil drive and function-gate timing signals are generated by the controller. The coil drive timing signals are sequenced on and off so as to start and stop the drive field in the proper phase. Data to and from the MBM(s) are transferred bit-serial. The signals STROBE, $\overline{\text{SYNC}}$, and SRCLK are provided to clock this data. Control timing is given in Figure 10 and Table 4.

Oscillator

An on-chip oscillator provides the internal time base to operate the controller when connected to an external crystal as shown in Figure 7. Alternatively, XIN can be driven from an external oscillator and XOUT not used. The crystal or external oscillator frequency is 64 times the coil drive frequency.

Reset and Power-Down

The $\overline{\text{RESET}}$ pin provides internal preconditioning of

the controller logic on power-up or other system reset conditions and also acts as a power-down interrupt which provides an orderly termination of any operation in progress with no loss of data in the MBMs.

$\overline{\text{RESET}}$ initializes the registers as follows (hexadecimal values):

LPC:	0000	
CMDR:	FF	(TERMINATE)
MSR:	01	
SAR:	0000	
RCR:	00	
SFR:	00	
STR:	C1	(while $\overline{\text{RESET}}$ is active)
	01	(after $\overline{\text{RESET}}$ is removed)

The system must be initialized after a reset to synchronize the MBM(s) with the controller. The user should load the SFR according to the system configuration, and then execute an INITIALIZE command.

When $\overline{\text{RESET}}$ is brought low, the controller ensures that all control pulse and coil drive signals are properly sequenced to the off condition so that no data is destroyed in the MBMs. This will occur within three magnetic cycles after $\overline{\text{RESET}}$ goes low. Data being written will usually not have been swapped in, and will have to be rewritten when the system is restarted. Note that if $\overline{\text{RESET}}$ is generated due to detection of low DC voltage, the power supply voltages may already be out of their specified operating ranges, and proper MBM operation may not be guaranteed. The user should provide input power detection or other means of sustaining DC voltages to minimize the chance of data loss.

Error Detection and Correction

In order to ensure the integrity of the data stored in the bubble memory system, the controller employs error detection and correction circuitry which operates automatically, and is in general transparent to the user.

During a normal WRITE DATA operation, the controller calculates and appends a 12-bit error correction code (ECC) field onto each block of 512 bits (64 bytes) written. Extra minor loops are provided in the MBMs for this field. The ECC used is a Fire Code which permits the identification and correction of any single burst of errors up to three bits long.

During a READ DATA operation, the controller recalculates the ECC field to verify the data. If an error is detected, the controller stops (provided the Stop on Error bit is set) and indicates the error in the status register. It also saves the ECC syndrome and data block address to enable re-reading (and error correction) of the erroneous block.

Two types of errors can occur:

1) Soft errors — due to transient phenomena in the detection and sense circuitry. The data in the memory is good and can usually be re-read correctly.
2) Hard errors — due to incorrect data in the MBM(s). The READ CORRECTED command rereads the erroneous block and sends corrected data to the user in most cases. The data should then be re-written to the MBM(s) to correct the memory contents.

Soft and uncorrectable errors are detected and indicated only by the READ CORRECTED command. If an error is detected during a READ DATA command with Stop on Error set, the controller saves the calculated ECC syndrome. The READ CORRECTED command uses two separate ECC circuits: one attempts to do error correction using the error syndrome, the other recalculates the syndrome on the raw data received from the MBM(s). This recalculated syndrome is compared to the saved syndrome from the READ DATA. If they are not equal, the Soft Error bit is set indicating that the data reread was *not the same as the originally-read data.* If the error-*correction* circuit does not find a correctable error, the Uncorrectable Error bit is set.

If a soft error occurs, the error-correction circuit cannot function properly. However it may have been "fooled" and changed some data. Therefore the data received during READ CORRECTED with a soft error indication should be ignored, and the data reread with the READ DATA command.

Hard errors are rare, and the block structure of the MBM, and interleaved operation of multiple MBMs causes most hard errors to be correctable, i.e. a hard failure in a single minor loop affects only one bit in any ECC block (except for a single MBM2256 system).

The controller also calculates and inserts an ECC field during a WRITE MAP operation. This field is checked during the INITIALIZE (L = 1) and READ MAP (C = 1) operations; however error correction is not performed for the map data.

The ECC details and capabilities are summarized in Table 5.

PROGRAMMING INFORMATION

Nine basic commands with 24 options provide total control of the bubble memory subsystem. The user stores a command into the command register, transfers data bytes as required, then checks the controller status to verify proper completion of the operation.

Registers

Eight registers are directly accessible by the user via the data bus. The desired register is selected by the three-bit address on A2–A0 when $\overline{\text{CS}}$ is true (low). (DATA can also be selected by $\overline{\text{DACK}}$.) All are read-write except the STR which is read only.

While a command is executing (READY = 0), writing is inhibited except to DATA and to CMDR bits 1&0; therefore only a Terminate (Immediate) command can be accepted (CMDR bits 7–2 will not be altered). The registers are summarized in Table 6.

Symbol (Address)	Name and Use
CMDR (000)	— Command Register — loaded by the user with the command to be exe-

cuted by the controller (see Commands).

MSR (001) — Multiple Sector Register — loaded by the user with the number (0 indicates 256) of sectors/pages to be read or written by the subsequent multiple sector READ DATA or WRITE DATA command (not used for single sector commands).

SARL (010) SARH (011) — Sector Address Register, two bytes, L = Low-order 8 bits, H = high-order bits — loaded by the user with the address of the (first) sector/page to be read or written by the subsequent (multiple sector) command.

RCR (100) — Residual Control Register — selects various options which apply to subsequent commands. Individual bits provide specific options as follows:

Bit	Function
7	Not used, always zero.
6	Read Buffer Enable — used primarily for diagnostic functions. This bit must be set to 1 if it is desired to read from the data buffer when no command is in progress. Otherwise, the buffer may be written into, but not read from. For proper operation, it must be reloaded with a 0 before initiating a subsequent command. 0: Buffer is write-only between commands. 1: Buffer is read-only between commands.
5	Stop on Error — causes the controller to terminate any READ DATA command at the end of any ECC block in which a data error was detected. The ECC logic, SAR, and MSR are left in the proper state for execution of a READ CORRECTED command.
4	Half Buffer — causes DRQ to be set only when the buffer is at least half full* (READ) or half empty (WRITE). When Half Buffer is set to 1, data may be transferred in 8-byte bursts in response to DRQ. The setting of DRQ according to Half Buffer and the number of bytes in the buffer is as follows: HB READ WRITE 0: ≥ 1 byte ≤ 15 bytes 1: ≥ 8 bytes* < 8 bytes *or at end of command if buffer is not empty.
3	Enable READY Interrupt — causes INT to be activated at the termination of any command. INT is cleared by reading STR or writing CMDR. May be set concurrently with bit 2.
2	Enable DRQ Interrupt — causes INT to be activated whenever DRQ is true. May be set concurrently with bit 3.
1	Page Addressing Mode — (see Sector/Page Addressing)- 0: Sector Addressing Mode (default). 1: Page Addressing Mode.
0	Write Protect — prevents any WRITE command from being executed. A write protect error will be indicated if any WRITE (Map or Data) is attempted with Write Protect = 1.

SFR (101) — System Features Register — defines the system configuration. Functions of the individual bits are as follows:

Bit	Function
7-3	Not used, always zero.
2	External Map — indicates that all map data is to be stored or is pre-stored in the external map memory (RAM or PROM). The controller does not use its internal map storage.
1, 0	Bank Size — specifies the number of MBMs in the active bank as follows: 00: 1 MBM, 01: 2 MBMs, 10: 4 MBMs, 11: 8 MBMs

STR (110) — Status Register (Read Only) — indicates the status of the command in progress or last ended — cleared when CMDR is loaded (except TERMINATE when busy) or by $\overline{\text{RESET}}$. Certain bits pertain only to specific commands or are defined differently for different commands. The meanings of the bits are as follows:

Bit	Command	Meaning
7	RDC	Soft Error — the recomputed ECC syndrome did not match the previous syndrome (see Error Correction/Detection).
6	WRD,WRM	Write Protect bit is set — command not executed.
7&6	—	$\overline{\text{RESET}}$ pin is active (low).
5	RDD,WRD	Sector/page Address Out of Range for the number of MBMs specified.
	RDM (C = 1)	Map compare error — the data read from the

		MBM(s) did not match that in the map memory.
	INIT	Initialization error — synchronization pattern could not be found.
4	RDC	Non-correctable error.
3	all READS	Data Error detected (ECC). For RDC command, indicates that error is in a different block than previous error.
2	all READS and WRITES	Data Buffer overrun — the user did not read/write the data buffer fast enough to keep up with the MBM data transfer rate, or the user attempted to read/write the buffer when DRQ = 0.
1	all RD & WR	Data transfer request (DRQ).
0	all	Ready — previous command has terminated and controller is ready to receive a new command.
DATA (111)		Data buffer — a 16-byte first-in-first-out (FIFO) buffer used for all data transfers.

Sector/Page Addressing

A *page* of data corresponds to a single physical read or write of the MBM(s) — therefore, the page length is determined by the MBM type (256K or megabit) and the number of MBMs specified in the SFR. The number of pages in a bank is independent of the number of MBMs, and is determined only by the MBM type.

Note: A minimum block size of 64 bytes is required for the ECC. Therefore, a single 256K-bit bank utilizes two physical pages per logical page.

A *sector* is a fixed-length record independent of the number of MBMs specified in the SFR and is equal to the maximum-length page for the MBM type. Therefore, the number of sectors in a bank is proportional to the number of MBMs.

Sector addressing is selected by default. Page addressing may be selected by setting the Page Mode bit = 1 in the RCR. Sector and page addressing are equivalent for a maximum bank of 8 MBMs.

Regardless of the mode or number of MBMs, error detection/correction is performed on blocks of 512 bits (64 bytes). In general, there are multiple ECC blocks within a sector/page.

Table 7 shows the sector and page sizes and counts for all configurations.

Logical Addressing

Propagation of the bubbles along the input or output track causes the data loops to be shifted an equal distance. Thus, following a replicate and clearing of the output track, the physically adjacent page has propagated well past the replicate gates; a similar affect occurs during consecutive writes. In order to provide minimum access time when reading or writing consecutive pages/sectors, the controller uses a logical addressing scheme such that consecutive logical pages are spaced several physical locations apart to account for the latency described above. This spacing is given in Table 8.

The controller maintains the current logical page/sector address in the Logical Page Counter (LPC), a non-accessible register which is incremented by the appropriate value during each active MBM cycle. The LPC is compared to the SAR to locate the desired page/sector for READ & WRITE commands. To synchronize the LPC with the MBM contents, the INITIALIZE or CLEAR LPC command should be used. $\overline{\text{RESET}}$ also clears the LPC to zero regardless of MBM position.

The timing of the WRITE DATA command is such that consecutive commands to consecutive logical addresses (without reloading the SAR) will be accomplished with minimum latency. During a multiple-page/sector READ DATA command, replicates are performed "on the fly" as each logical page reaches the replicate position; however the extra propagation distance between the replicate gates and the detector means that at the termination of a READ DATA command, the next logical address has passed the replicate position. The POSITION READ command will give minimum access time when consecutive logical pages/sectors are to be read with single-page/sector commands.

Commands

The user initiates operation of the controller by writing a command byte into the command register (CMDR). The various commands are described below and summarized in Table 6. For each command, the value to be loaded into the CMDR is given in binary with certain option bits which affect its operation. Use of the SAR and MSR is described where applicable. These registers, when used, as well as the SFR and RCR, must be loaded prior to loading the CMDR.

Data Transfer

All data transfers are made to/from the data buffer which is accessed as register 7. During a read or write command execution, when the controller determines that a data transfer is required, it does the following:

1) sets the DRQ bit in the status register.
2) raises the DRQ pin to the active (high) state.
3) if RCR bit 2 (Enable DRQ Interrupt) is set, raises the INT pin to the active (high) state.

Any of these conditions may be recognized by ap-

propriate software or hardware as indicating that data transfer is required. The user then transfers one or more bytes to or from the buffer using $\overline{WR}$ or $\overline{RD}$ and either of the following:

1) addressing Register 7 ($\overline{CS}$ = 0, A2,A1,A0 = 111).

2) activating $\overline{DACK}$ ($\overline{CS}$ = 1, $\overline{DACK}$ = 0, A2–A0 ignored).

The DRQ and $\overline{DACK}$ signals may be used with a separate direct memory access (DMA) controller. DRQ and INT (if used) remain active as long as data transfer is required.

If the RCR Half Buffer bit is set to 1, then eight bytes can always be transferred in a burst when a DRQ occurs.

Notes:

The WRITE DATA (S = 0) AND WRITE MAP commands do not begin execution until the first data byte has been written into the data buffer. When using programmed data transfer, the user should always load the first 16 data bytes in a burst as fast as possible so as to provide adequate buffering for the operation. (It is not necessary to check DRQ since the buffer is known to be empty at the start of the command.)

Due to the asynchronous operation of the data buffer, the controller always attempts to keep it full during a write operation. As a result, it may request up to 16 additional bytes at the end of a write depending on the user system response time. Response to these extra DRQs is optional: extra bytes transferred will not be written to the MBM(s); ignoring the DRQ will not cause an error.

Termination and Status

When the command execution is finished, the controller:

1) sets the Ready bit and any other bits which are appropriate in the status register.
2) if RCR bit 3 (Enable Ready Interrupt) is set, raises the INT pin to the active (high) state.

The user should read the status register to verify proper completion of the previous command and take any corrective action indicated. Ready indicates that the controller is able to accept a new command.

INT, if used, is cleared by reading the status register or loading the command register.

Command Descriptions

INITIALIZE (INIT) CMDR = 1111 L100

Read the map loop until the synchronization pattern (64 ZEROs followed by a ONE is detected, then set the logical page counter (LPC) to zero. Then if L = 1, load the redundancy map memory with the map data.

If the synchronization pattern is not found after one complete cycle of the map loop, the map loop is shifted one position and a second attempt is made reading the interleaved bits.

INITIALIZE should be executed after any of the following:

1) Power off-on.
2) Reset.
3) Bank switching or MBM change.

Page synchronization is then maintained until any of the above conditions occurs. The Load Map Memory (L = 1) option should be used unless it is not desired to use the redundant-loop map or the map has been prestored in an external PROM.

Register usage: None.

Errors detected:

Initialization error — the synchronization pattern could not be found on either pass.

Data error — an ECC error was detected when reading the map data.

CLEAR LPC (CLPC) CMDR = 0010 0000

Clear the Logical Page Counter (LPC) to zero without accessing the MBM(s) or loading the map memory. Permits the user to synchronize the controller to sector/page zero without using the map loop(s), e.g. by recognizing a page with a unique data pattern.

Useful in systems where the map data are stored in an external PROM and the bulk erase capability of the MBM is utilized, since bulk erase will destroy the synchronization pattern along with the data.

POSITION (POS) CMDR = 0W10 1000

Position the MBM data for minimum access time for a subsequent READ DATA (W = 0) or WRITE DATA (W = 1) command. RDD and WRD will automatically position the MBM(s) if required; POS minimizes the latency at the time the RDD or WRD is executed.

Register Usage:

Start: SAR: Address of sector/page to be read or written by a subsequent command.

End: SAR: Unchanged. **The SAR should not be reloaded prior to issuing the RDD or WRD command, even with the same address, or the effect of POS will be lost and the RDD or WRD access time will be excessive.**

WRITE DATA (WRD) CMDR = 010M US00

Write one or more sectors/pages of data. Positioning is performed if the MBM(s) have not been pre-positioned.

M = 0: Write one sector/page.

M = 1: Number of sectors/pages is specified in MSR.

U = S = 0: Normal Write — user sends only data bits; zeros are inserted for redundant loops, and ECC bits are generated and appended.

U = 1,S = 0: Unmasked Write — user sends data for all loops including redundant and ECC bits.

U = 0,S = 1: Suppress Transfer — the 16 bytes currently in the buffer are written repeatedly, with redundant loop and ECC bits inserted as in a normal write; the user does not send data.

U = S = 1: NOT ALLOWED.

Register Usage:

Start: SAR: Address of (first) sector/page to be written.
MSR: M = 0: Not used.
M = 1: Number of sectors/pages to be written.

End: Norm: SAR: Address of last sector/page written + 1.
MSR: M = 0: Unchanged.
M = 1: MSR = 1.

Error: SAR: Address of the sector/page having the error.
MSR: M = 0: Unchanged.
M = 1: Number of sectors/pages still to be written including the one with the error.

Errors detected:

Write protect — write protect bit is set; WRD is not executed.

Out of Range — if the initial address is out of range, the command is not executed; if a command attempts to write past the end of the installed memory, the command terminates after the last allowable sector/page.

Overrun — the command is terminated immediately.

READ DATA (RDD) CMDR = 000M US00

Read one or more sectors/pages of data. Positioning is performed if the MBM(s) have not been pre-positioned.

M = 0: Read one sector/page.

M = 1: Number of sectors/pages is specified in MSR.

U = S = 0: Normal Read — redundant loops and ECC are masked and remaining bits are sent to the user; ECC is checked and errors reported.

U = 1,S = 0: Unmasked Read — all bits are sent to the user; ECC is not checked.

U = 0,S = 1: Suppress Transfer — data are not sent to the user; ECC is checked and errors reported.

U = S = 1: NOT ALLOWED (= RDC command).

Register Usage:

Start: SAR: Address of (first) sector/page to be read.
MSR: M = 0: Not used.
M = 1: Number of sectors/pages to be read.

End: Norm: SAR: Address of last sector/page read + 1.
MSR: M = 0: Unchanged.
M = 1: MSR = 1.

Error: SAR: Address of sector/page having the error.
MSR: M = 0: Unchanged.
M = 1: Number of sectors/pages still to be read including the one with the error.

Errors detected:

Out of Range — if the initial address is out of range, the command is not executed; if a command attempts to read past the end of the installed memory, the command terminates after the last allowable sector/page.

Data Error (ECC) — if Stop on Error is set, data transmission to the user stops immediately following the 64-byte ECC block in which the error is detected.

Overrun — the command is terminated immediately.

READ CORRECTED (RDC) CMDR = 0000 1100

Reread the page in which an error was detected and apply error correction to the erroneous block. Only valid immediately following a READ DATA command with a Data Error indication and with the Stop On Error bit set in the RCR.

Corrected data are sent to the user starting at the beginning of the 64-byte ECC block in which the error was detected and continuing to the end of that sector or page; i.e. the last 64 bytes sent by the RDD are repeated with error correction, and the sector or page is completed. A soft or uncorrectable error in the first block or a data error in a subsequent block will be indicated if detected, but the sector/page will be completed regardless of errors or the Stop On Error bit. See *Error Detection and Correction.*

Register Usage:

Start: No registers may be loaded between the end of READ DATA and the issuing of READ CORRECTED.

End: Norm: SAR: Address of next sector/page.
MSR: Remaining sector/page count.

Error: SAR & MSR: Unchanged.

Errors detected:

Soft error — the recalculated ECC syndrome did not match the saved syndrome.
Uncorrectable error — the error was not correctable.
Data error — an error was detected in another ECC block.
Overrun — the command is terminated immediately.

TERMINATE (TERM) CMDR = XXXX XX11

Terminate the current operation at the end of the current page (I = 0) or terminate immediately (I = 1). TERMINATE permits aborting of any command in progress at any time.

If the controller is not busy, TERMINATE is treated as a no-op, except for resetting the buffer pointers.

Register Usage: Buffer (FIFO) pointers are reset.

Errors detected: Depends upon the command being executed.

READ MAP (RDM) CMDR = 1000 C000

Read the map loop data and send to the user. The order of the data read is as shown in Table 3 grouped into 8-bit bytes with the first bit being the most-significant bit in the byte. In a multiple-MBM system, bits from the MBMs are interleaved.

C = 0: The entire map loop contents (64 or 128 bytes) are sent to the user. Error detection is not performed.

C = 1: Check Data — only the M-field and ECC-field are sent to the user; ECC checking is performed, and the map data (M-field) are compared to the contents of the map memory. Errors are reported.

Register usage: none.

Errors detected:

Map compare error (C = 1 only) — the data read from the map loop did not match that stored in the map memory.
Data error (C = 1 only) — an ECC error was detected (map error correction is not performed by the controller).
Overrun — the command is terminated immediately.

WRITE MAP (WRM) CMDR = 1100 N000

Write map loop 1 (N = 0) or 2 (N = 1) with user-supplied data. The user must supply the entire map loop contents (64 or 128 bytes per MBM) including the sync pattern as described under READ MAP. However, the ECC-field bits are ignored and replaced by ECC bits generated by the controller.

Register usage: None.

Errors detected:

Write protect — the write protect bit is set; WRM is not executed.
Overrun — the command is terminated immediately.

Note:
WRITE MAP will execute in a multiple-MBM system but will not generate correct ECC bits for multiple MBMs. It is intended for loading the map in a single MBM only. The MBM must first be erased using the Z-coil or a suitable external magnetic field. The MBM map pins must be connected as shown in Figure 6.

TABLE 1. BUBBLE MEMORY CAPACITIES

	MBM2256	MBM2011
Number of data loops:	282	584
Number of redundant loops:	20	60
Number of loops used for ECC:	6*	12
Number of usable data loops:	256	512
Number of bits per loop:	1024	2048
Number of bits of data storage:	262,144	1,048,576
Number of map loops:	2	2
Number of bits used in map loops:	512	1024

* Actually 12 bits in every other physical page.

TABLE 2. EXTERNAL MEMORY REQUIREMENTS

MBM Type	Number of MBMs	External Memory Required (bits) SFR bit 2 = 0	1
2256	1	0	282
	2	0	564
	4	534	1128
	8	1662	2256
2011	1	0	584
	2	574	1168
	4	1742	2336
	8	4078	4672

Minimum requirement; additional bits are not used.
Memory must be configured one bit wide.
Internal Map Memory capacity: 594 bits.

TABLE 3. MAP LOOP FORMAT

Pattern:	Field	Number of bits		Note
		256K	1M	
MM --- MM	Map Data	282	584	(1)
EE --- EE	ECC	12	12	(2)
UU --- UU	User	152	362	(3)
00 --- 001	Sync	65	65	(4)
X	X	1	1	(5)

(1) Each bit marks the corresponding data loop:
M = 1: good loop.
M = 0: redundant loop.
For correct operation, there should be exactly 262 (256K) or 524 (1M) 1s in this field.

(2) Error Correction (Fire) Code — applies only over the Map Data field.

(3) May be used for any purpose such as an identification number. However, it must not contain any sequence of 64 zeros followed by a one. Such a pattern will be recognized as a sync pattern and cause incorrect initialization.

(4) Synchronization pattern — 64 ZEROs followed by a ONE.

(5) This bit is skipped after synchronization is established before reading the first Map Data bit.

TABLE 4. NOMINAL CONTROL PULSE TIMING

Pulse	256 K		MEGABIT	
	Start	Width	Start	Width
XA	33	31	33	31
shut down	12	—	12	—
XB	1	31	1	31
start up (XB off)	46	—	46	—
YA	49	31	49	31
YB	17	31	17	31
start up (YB off)	62	—	62	—
shut down	60	—	60	—
GEN	17	2	17	2
SWAP	53	63	53	63
MAP TR-IN (SWAP pin)	53	39	53	39
CUT	0	3	63.5	2
REP	1	20	1	18
RMAP	1	20	1	18
STROBE	34	12	34	12
$\overline{\text{SYNC}}$	0	4	0	4
SRCLK	0,8, . . .	4	0,8, . . .	4
$\overline{\text{CLRMAP}}$	0	46	0	46
CLKMAP	0,8, . . .	4	0,8, . . .	4
$\overline{\text{WRMAP}}$	3,11, . . .	4	3,11, . . .	4

1 unit = 1 oscillator cycle.
= 1/64th magnetic cycle.
= 5.625 degrees of rotation.
= 125 ns at 125,000 bits per second.
= 156.25 ns at 100,000 bits per second.

REFERENCE: SRCLK zero (0) transition.
All times ± 50 ns except:
$\overline{\text{SYNC}}$, $\overline{\text{CLRMAP}}$, CLKMAP: +100 / − 0 ns

TABLE 5. ERROR CORRECTION CODE SUMMARY

Type of code:	Fire Code.
Generator polynomial:	$(x^5+1)\cdot(x^7+x^6+x^5+x^4+x^2+x+1)$
No. of data bits per ECC block:	512 (282 or 584 for Map loop)
No. of check bits per ECC block:	12
Total bits per block:	524 (294 or 596 for Map loop)
Correctable errors:	any burst of 1 to 3 bits.

Redundant loop bits and interleaved zeros in the map field are not included in the ECC operation.

TABLE 6. REGISTER AND COMMAND SUMMARY

Addr	Reg.	Reset
0	CMDR	FF
1	MSR	01
2	SARL	00
3	SARH	00
4	RCR	00
5	SFR	00
6	STR	01*
7	DATA	—

Cmd.	Byte	Option bits
RDD	0 0 0 M U S 0 0	M = Multiple
RDC	0 0 0 0 1 1 0 0	U = Unmasked
WRD	0 1 0 M U S 0 0	S = Suppress transfer
POS	0 W 1 0 1 0 0 0	W = Write position
RDM	1 0 0 0 C 0 0 0	C = Check data
WRM	1 1 0 0 N 0 0 0	N = Loop #2
INIT	1 1 1 1 L 1 0 0	L = Load map memory
CLPC	0 0 1 0 0 0 0 0	
TERM	- - - - - - 1 1	I = Immediate

* = C1 while $\overline{\text{RESET}}$ is active.

Bit	SFR	RCR	STR	(applicable command)
7:	0	0	Soft Error	(RDC)
6:	0	Read Buffer Enable	Write Protect	(WRD,WRM)
5:	0	Stop on Error	Out of Range	(RDD, RDC, WRD)
			Map Compare Error	(RDM)
			Initialization Error	(INIT)
4:	0	Half Buffer	Non-Correctable Error	(RDC)
3:	0	Enable READY Interrupt	Data Error	(all RD, INIT)
2:	External Map	Enable DRQ Interrupt	Overrun	(all RD/WR)
1:	$\log_2$	Page Mode	DRQ (data request)	(all RD/WR)
0:	# MBMs	Write Protect	Ready	(all)

TABLE 7. SECTOR AND PAGE SIZES

MBM	Number of MBMs	Sector		Page	
		Length (Bytes)	Number of Sectors	Length (Bytes)	Number of Pages
2256	1	256	128	64*	512
	2	256	256	64	1024
	4	256	512	128	1024
	8	256	1024	256	1024
2011	1	512	256	64	2048
	2	512	512	128	2048
	4	512	1024	256	2048
	8	512	2048	512	2048

* A minimum block size of 64 bytes is required for the ECC. Therefore, a single 256K-bit bank utilizes two physical pages per logical page.

TABLE 8. PAGE SEPARATION AND LATENCY

	256 K	MEGABIT	UNITS
Physical page length:	282	584	bits
Inter-page gap:	15	17	bits
Logical page separation:	297	601	bits
Page transfer time (incl. gap):	297 (1)	601	cycles
Read and write latency (2)			
READ DATA (RDD)			
after POSITION READ (3)	181	92	cycles
after RDD, next logical address	1024	2048	cycles
random address { min:	463	676	cycles
{ max:	1486	2723	cycles
WRITE DATA (WRD)			
after POSITION WRITE (3)	0	0	
after WRD, next logical address (3)	0	0	
random address { min:	1	1	cycle
{ max:	1024	2048	cycles
User peak data transfer rate (4)			
@ 125 kHz:	N*15,625		bytes/sec
@ 100 kHz:		N*12,500	bytes/sec

(1) 594 cycles for single MBM2256 (2 physical pages).

(2) Number of MBM magnetic cycles before MBM data transfer begins — there is an additional overhead delay in the controller of between three and four cycles from the loading of the CMDR (RDD) or first data byte (WRD).

(3) Provided that the SAR is not reloaded between commands.

(4) @ Field frequency. N = number of MBMs operating in parallel. This is the peak burst rate; average rate is reduced by the ratio of the number of bits transferred to the total page transfer time.

FIGURE 2 — MAGNETIC BUBBLE MEMORY FUNCTIONAL DIAGRAM

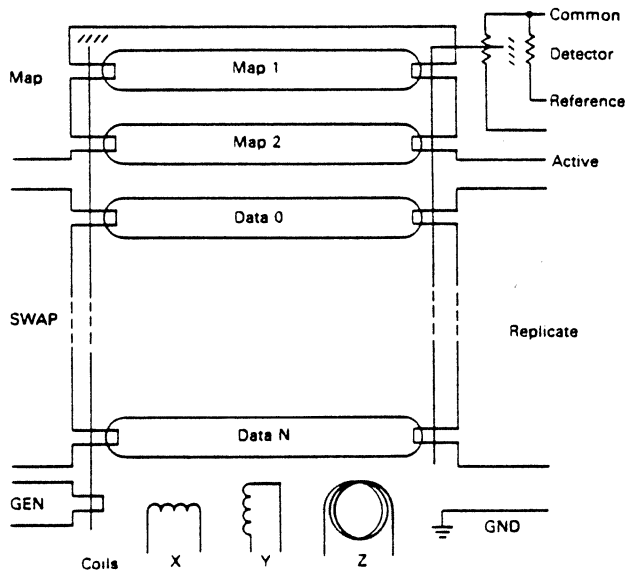


FIGURE 3a — SINGLE-MBM SYSTEM

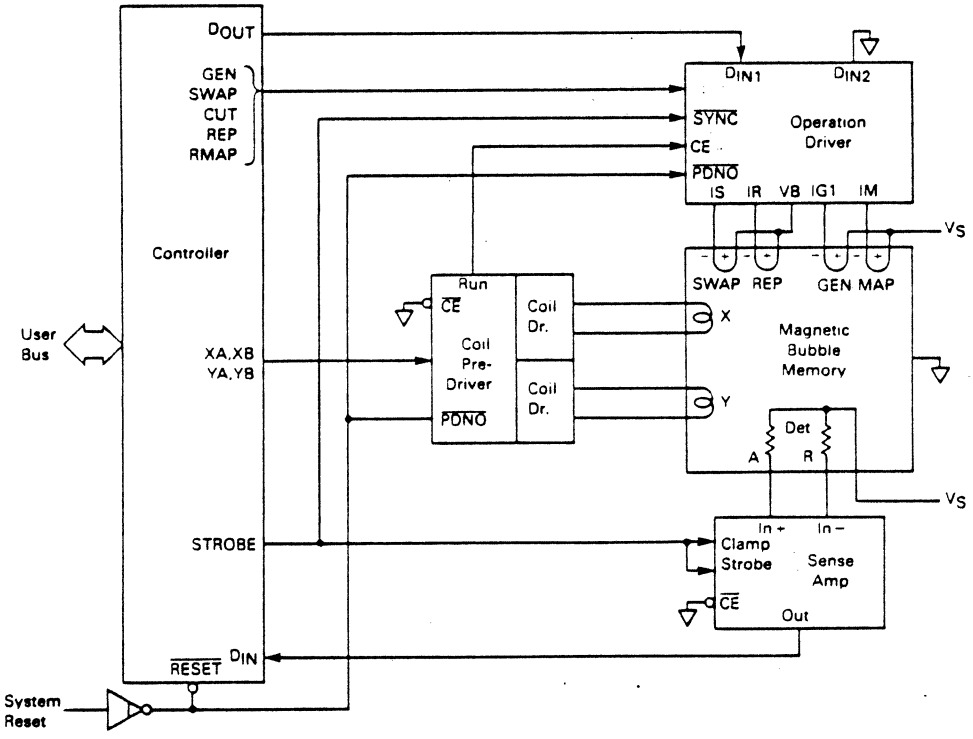


FIGURE 3b — MULTIPLE-MBM SYSTEM

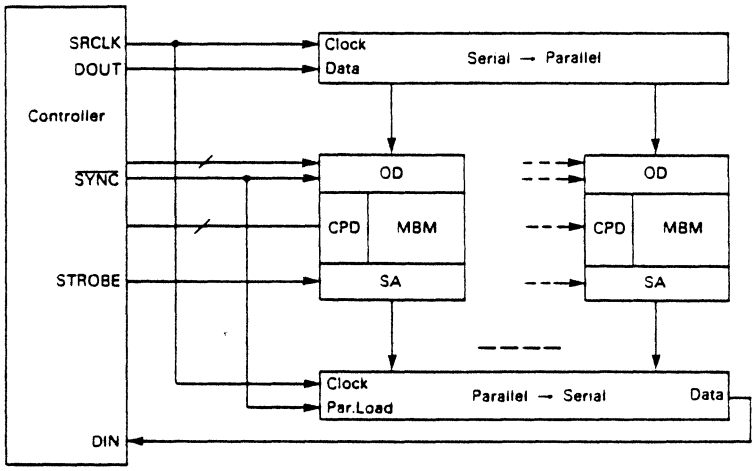


FIGURE 3c — MULTIPLE-BANK SYSTEM

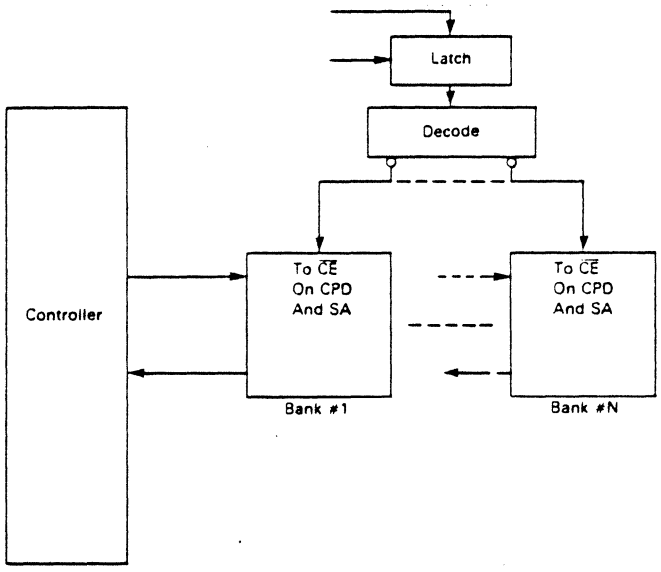


FIGURE 4 — EXTERNAL MAP MEMORY CONNECTION

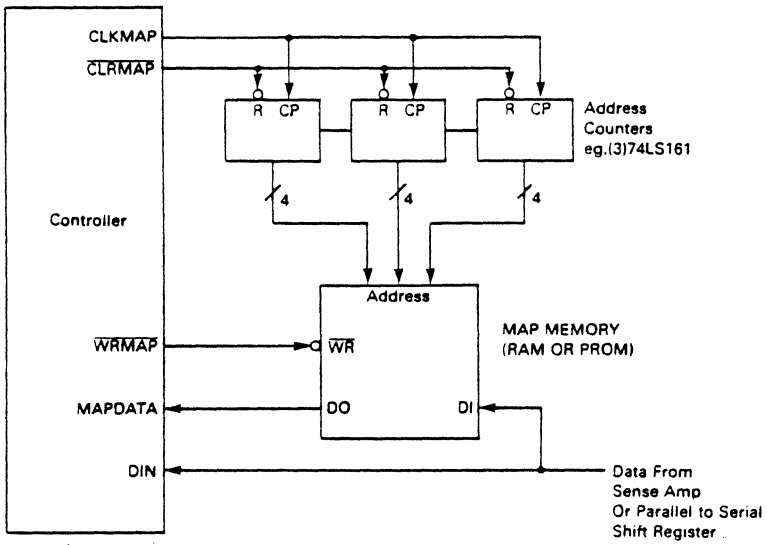


FIGURE 5 — CONTROLLER BLOCK DIAGRAM

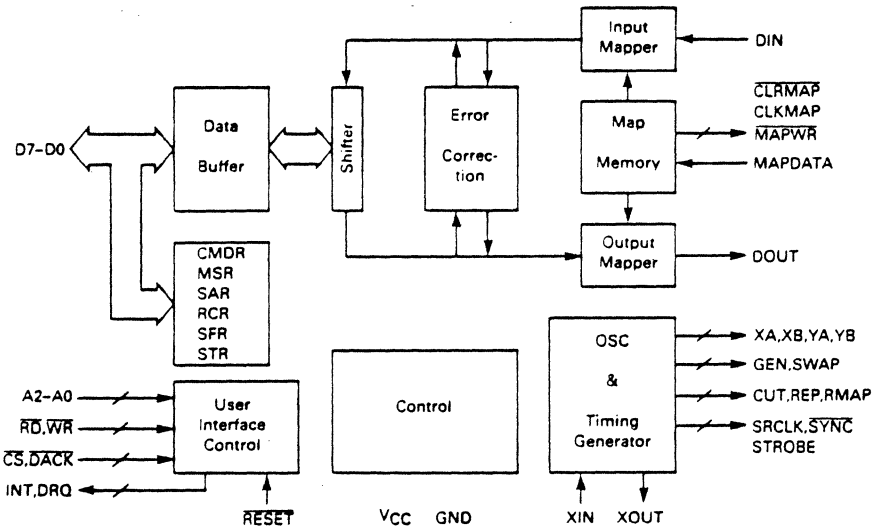


FIGURE 6 — MAP WRITE SWITCH

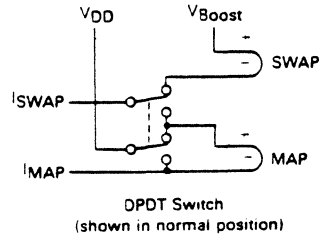


FIGURE 7 — CRYSTAL OSCILLATOR CIRCUIT

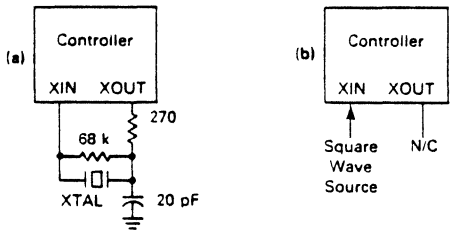


FIGURE 8 — USER INTERFACE TIMING

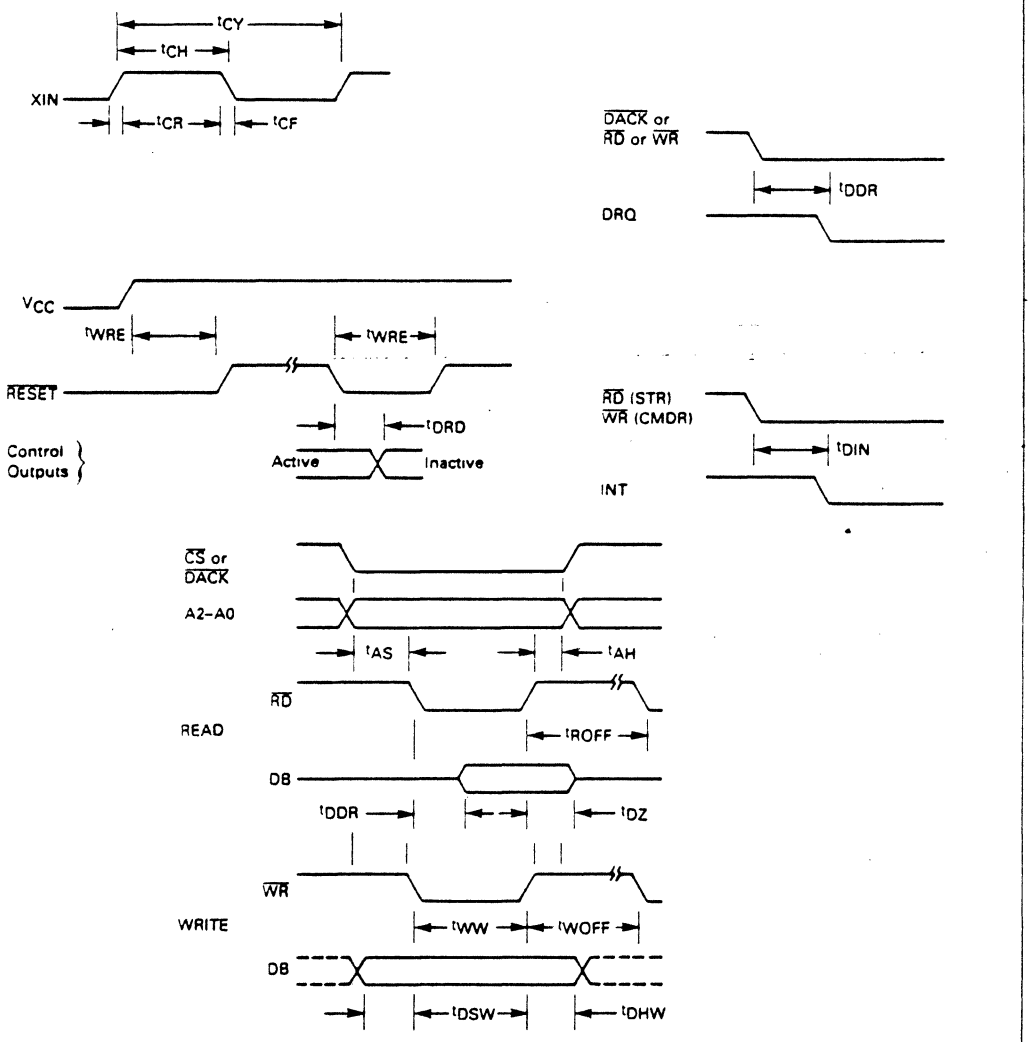
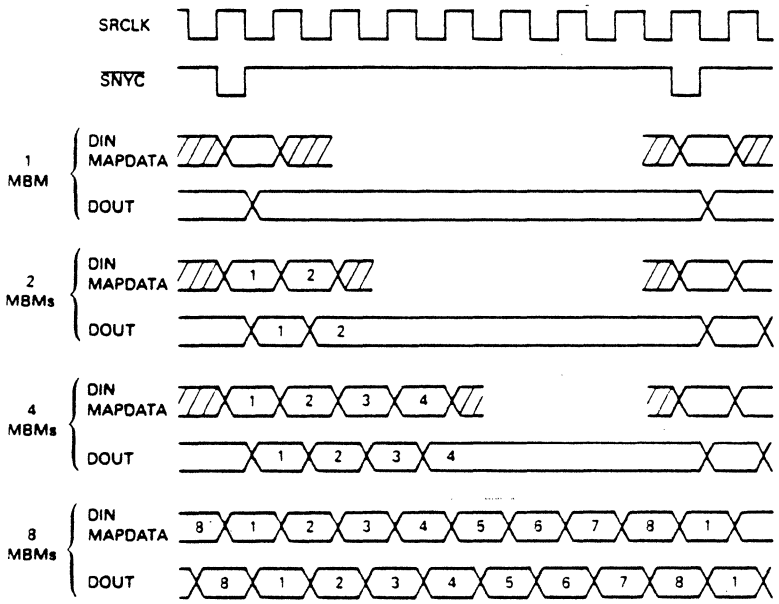


FIGURE 9 — DIN, DOUT, AND MAP MEMORY TIMING



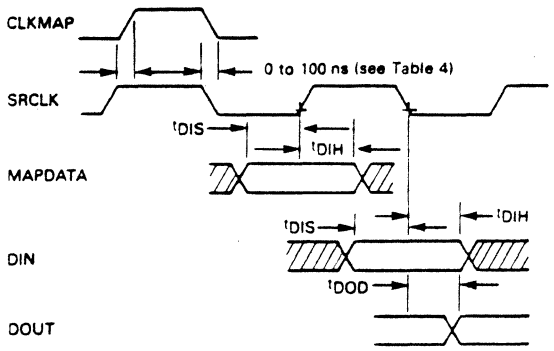
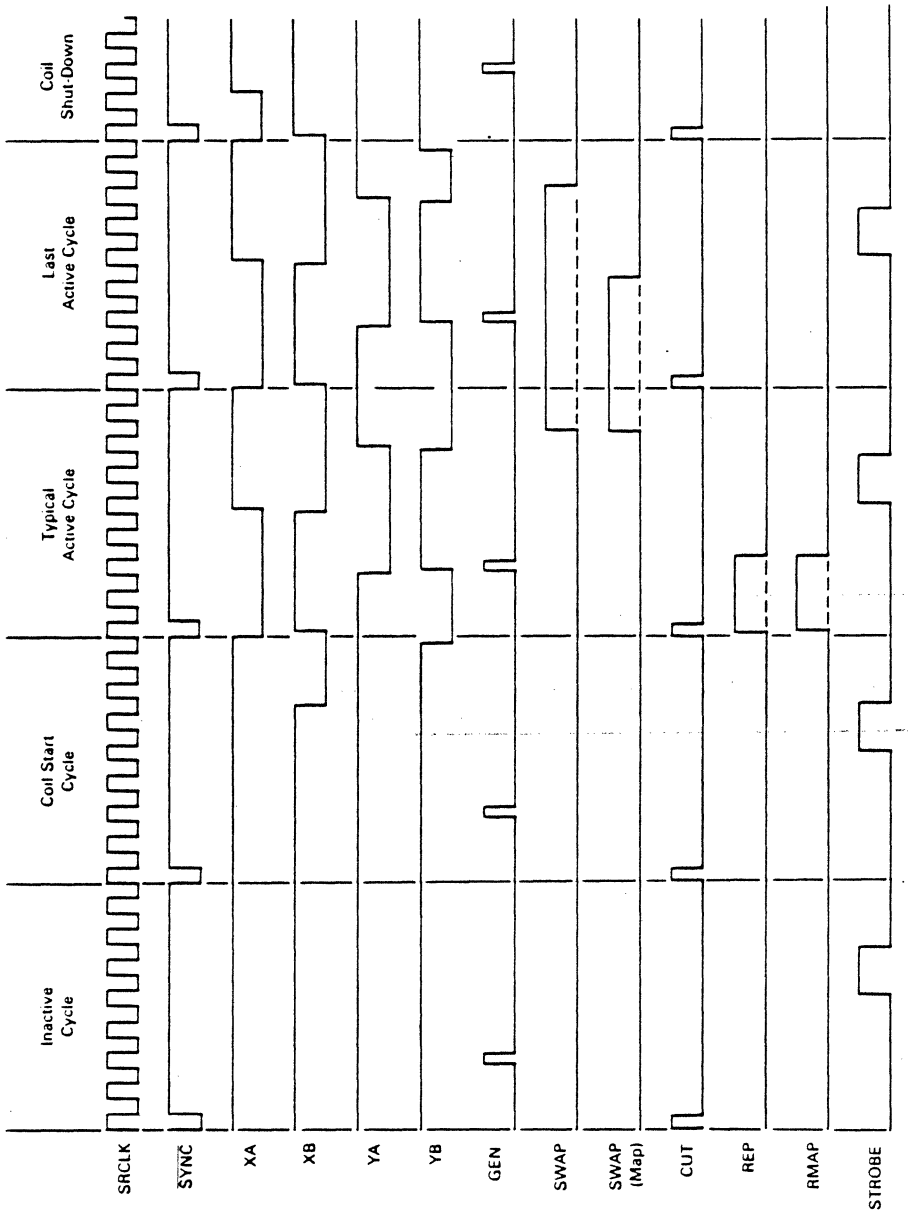


FIGURE 10 — CONTROL SIGNAL TIMING



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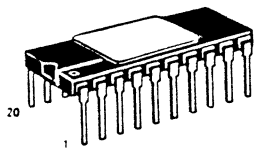
BUBBLE MEMORY PRODUCTS

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SC42468

Advance Information

BUBBLE MEMORY COIL PREDRIVER



GENERAL DESCRIPTION

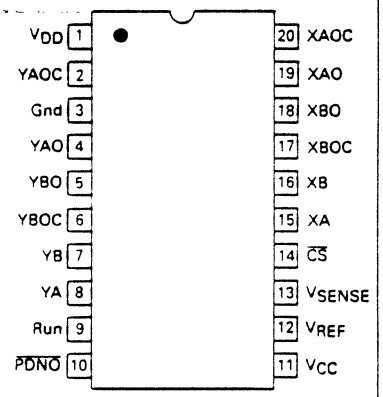
THE SC42468 Bubble Memory Coil Pre-driver is a monolithic CMOS integrated circuit which generates control signals for driving the X and Y field coils of a magnetic bubble memory device. The coil currents are switched through bridge configurations of complementary MOS Power FETs which are packaged separately. Basic control/timing signals are input to the coil pre-driver from the bubble memory controller.

The Coil Pre-driver also contains under-voltage sensing circuits for the two bubble memory system power supply voltages. These circuits provide an interlock signal which can be used to provide an orderly shut-down so as to prevent loss of data in the event of a loss of D.C. power. The SC42468 is packaged in a 20-pin dual in-line package.

FEATURES

- Level Shift from TTL to Coil Drive Voltage
- High Load-Capacitance Drive Capability for Low-On-Resistance Power FET Coil Drivers
- Coils Grounded When not Operating
- Interlock Disables Operation Driver When Coils are not Being Driven
- Under-Voltage Detection and Interlock
- Chip Select Input for Multiple-Bubble Systems

PIN ASSIGNMENTS



20-pin Dual In-line
Package: 0.3-inch row spacing

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Value	Unit
Storage Temperature	−65 to +150	°C
Ambient temperature with power applied Commercial Device Extended-temperature Device	 0 to +70 −55 to +125	 °C °C
Voltage — V_{DD} and Coil Drive Outputs	−0.5 to +15	Volts
Voltage — any other pin to GND	−0.5 to +7.0	Volts
Output Driver Current	180	mA
Power dissipation	1.2	Watts

*Absolute Maximum Ratings indicate limits beyond which permanent damage may occur to the device. Proper operation of the device requires that it be limited to the conditions specified under DC Electrical Characteristics.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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PIN DESCRIPTIONS

Inputs

$\overline{CS}$ — Chip Select — enables operation of the coil pre-driver.

XA — X coil positive current enable.

XB — X coil negative current enable.

YA — Y coil positive current enable.

YB — Y coil negative current enable.

Supplies and Miscellaneous

V_{DD} — Coil driver supply voltage.

V_{CC} — Logic supply voltage.

V_{REF} — Reference voltage for sensing circuits.

V_{SENSE} — V_{DD} sensing input.

GND — System Ground.

Outputs

XAO — X-coil positive-current N-channel driver enable.

XAOC — X-coil positive-current P-channel driver enable.

XBO — X-coil negative-current N-channel driver enable.

XBOC — X-coil negative-current P-channel driver enable.

YAO — Y-coil positive-current N-channel driver enable.

YAOC — Y-coil positive-current P-channel driver enable.

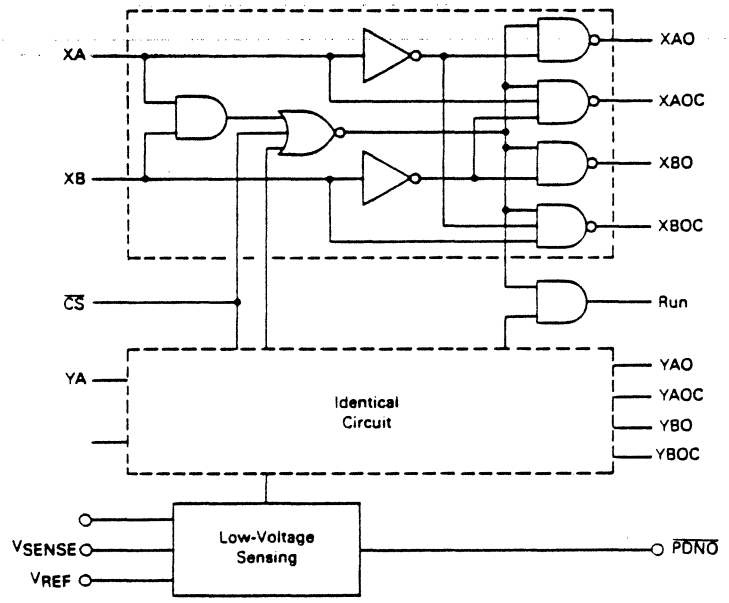
YBO — Y-coil negative-current N-channel driver enable.

YBOC — Y-coil negative-current P-channel driver enable.

RUN — Indicates that the X and Y coils are being driven — enables the operation driver.

$\overline{PDNO}$ — Power Down Output — indicates that at least one of the power supply voltages is below its minimum operating value.

FIGURE 1 — FUNCTIONAL DIAGRAM



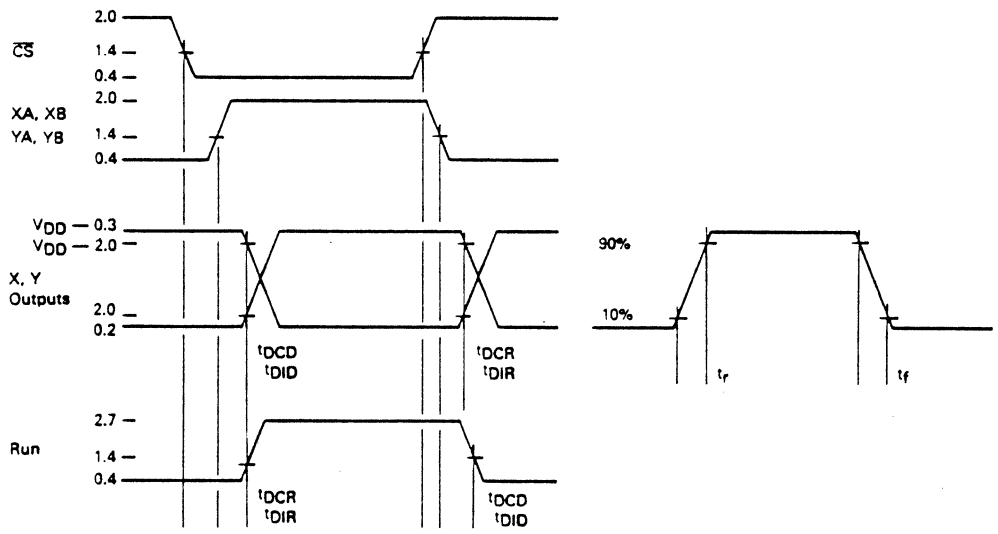
DC ELECTRICAL CHARACTERISTICS (V_{REF} = 2.50 V ± 1%, T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Coil Supply Voltage	V_{DD}	9.0	14.5	Volts
Logic Supply Voltage	V_{CC}	4.75	5.25	Volts
Current from V_{DD} (V_{DD} = 12.0 V, $\overline{CS}$ = 0)	I_{DD_1}	—	TBD	mA
Current from V_{DD} (V_{DD} = 12.0 V, $\overline{CS}$ = 1)	I_{DD_2}	—	TBD	mA
Current from V_{CC} (V_{CC} = 5.25 V)	I_{CC}	—	TBD	mA
Current from V_{REF} (V_{REF} = 2.525 V)	I_{REF}	—	TBD	μA
Logic High In Voltage (TTL)	V_{IH}	2.0	—	Volts
Logic Low In Voltage (TTL)	V_{IL}	—	0.8	Volts
Logic High Out Voltage (TTL) (I_O = −0.4 mA)	V_{OH}	2.7	—	Volts
Logic Low Out Voltage (TTL) (I_O = 1.6 mA)	V_{OL}	—	0.4	Volts
Logic High In Current (V_I = 2.7 V, V_{CC} = 5.0 V)	I_{IH}	—	20	μA
Logic Low In Current (V_I = 0.4 V, V_{CC} = 5.0 V)	I_{IL}	—	−40	μA
Driver High Out Voltage (CMOS) (I_{DOH} = −10 mA)	V_{DOH}	V_{DD} − 0.3	—	Volts
Driver Low Out Voltage (CMOS) (I_{DOL} = 10 mA)	V_{DOL}	—	0.2	Volts
Driver High Out Current	I_{DOH}	−250	—	mA
Driver Low Out Current	I_{DOL}	250	—	mA
Input Capacitance	C_{IN}	—	15	pF
V_{CC} Detection Threshold	V_{TCC}	TBD	TBD	Volts
V_{SENSE} Detect Threshold	V_{TS}	TBD	TBD	Volts
V_{CC} Power Up Enable	V_{ECC}	TBD	TBD	Volts
V_{DD} Power Up Enable	V_{EDD}	TBD	TBD	Volts

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 10.8 to 13.2 V, T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Output Rise Time (C_L = 450 pF)	t_r	—	35	ns
Output Fall Time (C_L = 450 pF)	t_f	—	35	ns
CS* to Driver Out (C_L = 450 pF)	t_{DCD}	—	300	ns
CS* to RUN Delay	t_{DCR}	—	300	ns
Other In to Driver Out (C_L = 450 pF)	t_{DID}	—	150	ns
Other In to RUN Out	t_{DIR}	—	TBD	ns

FIGURE 2 — SIGNAL WAVEFORMS



OPERATION

The magnetic bubble memory device requires a rotating magnetic field which is produced by the interaction of two orthogonal (X,Y) coils mounted inside the package. A uniform rotating field would be produced by driving the coils with sinusoidal currents displaced by 90° in time. In actual practice, an approximately triangular current waveform is produced by applying a voltage pulse to each coil through transistor switches and allowing the inductance of the coil to integrate the voltage into a current ramp. The pulse duration is small relative to the time-constant of the coil and series transistors so that the current ramp is approximately linear.

Timing inputs to the Coil Pre-driver are provided to the XA, XB, YA, and YB pins. These signals are active-high and enable the application of voltage pulses to the coil driver FETs, which in turn enable current flow in the coils. XA and YA enable positive current flow; XB and YB enable negative current flow. Four output drive signals are provided for each coil, one for each of the four switch transistors in the bridge (two P-channel, two N-channel). These correspond to the four inputs and their logical complements except that if both X(Y) inputs go high, all four X(Y) outputs go high. This is the off state wherein all N-channel drivers are turned on thus grounding both ends of both coils. When either coil is in the off state (XA = XB = high, or YA = YB = high), the RUN output is held low to disable the Operation Driver.

Note that the "X" and "Y" halves of the circuit are identical as are the "A" and "B" portions within each half. This symmetry may be taken advantage of to simplify printed-circuit board layout in some cases by interchanging "X" and "Y" or "A" and "B."

The Chip Select ($\overline{CS}$) input is active-low, and when false (high) overrides the timing inputs forcing the coil drivers into the off state, and places the Coil Pre-driver into a standby mode with reduced power consumption. Chip Select may be used to selectively enable one of a parallel-wired group of bubble memories, each with its own set of support circuits.

The Power Down ($\overline{PDNO}$) signal is active-low and goes low whenever either V_{CC} or V_{DD} drops below its normal operating range. V_{CC} is sensed internally, but since V_{DD} is variable (dependent on the operating frequency) it is sensed through the V_{SENSE} pin using a voltage divider (R_1 and R_2) from V_{DD}. At nominal V_{DD}, V_{SENSE} should be 2.90 volts. When power is applied, $\overline{PDNO}$ is held low until both V_{CC} and V_{DD} have reached their operating values. $\overline{PDNO}$ has an open-drain output and may be externally wired-ored.

FIGURE 3 — TYPICAL COIL WAVEFORMS
(X-COIL IDENTICAL, PHASE SHIFTED)
(1) ASSUMING X-COIL ALREADY BEING DRIVEN

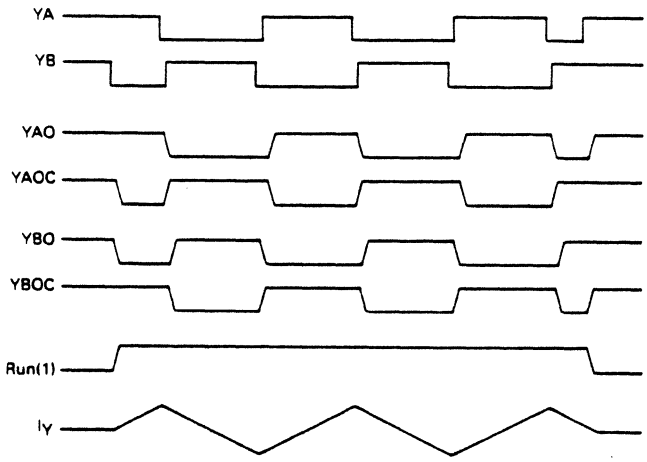
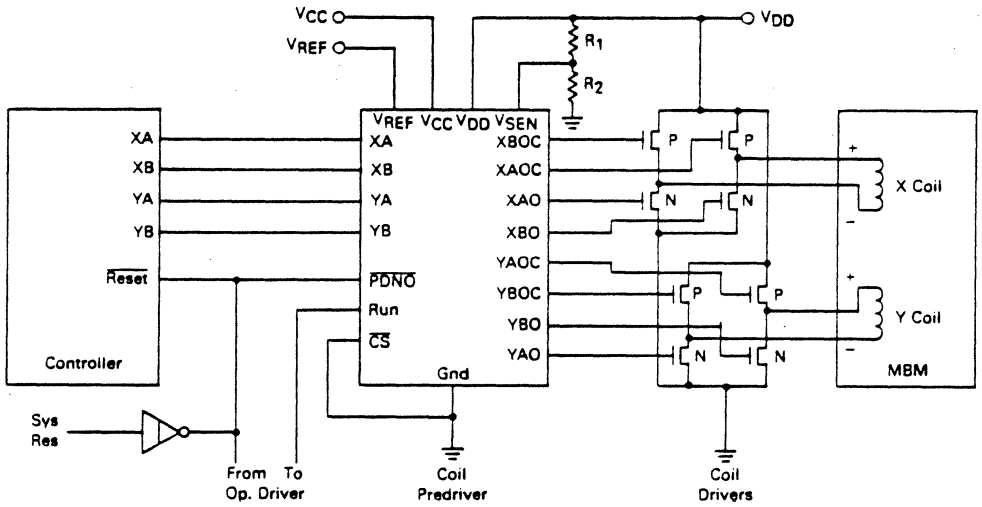


FIGURE 4 — TYPICAL APPLICATION



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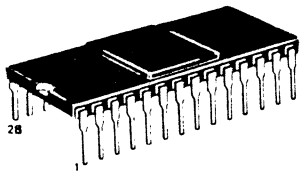
BUBBLE MEMORY PRODUCTS

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MC34046S
MC34047S

Advance Information

SINGLE BUBBLE MEMORY OPERATION DRIVERS



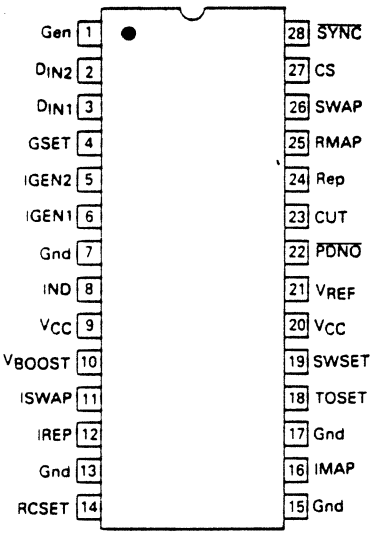
GENERAL DESCRIPTION

The MC34046S and MC34047S Single Bubble Memory Operation Drivers are monolithic bipolar linear integrated circuits which generate controlled-current pulses for the generate, swap, replicate and map-loop operations in a magnetic bubble memory device. The MC34046S and MC34047S are pin-compatible and specifically designed to drive the Motorola MBM2256 (256-kilobit) and MBM2011 (one-megabit) bubble memories respectively. They differ only in the amplitudes of the current pulses generated. Each Operation Driver can drive one bubble memory. Basic control/timing signals are input to the Operation Driver from the bubble memory controller. Each circuit contains a voltage booster to provide the high-voltage required by the swap and replicate circuits. Under-voltage detection prevents operation until this supply has reached its proper level. The circuits are packaged in 28-pin, 0.6-inch wide dual in-line packages.

FEATURES

- Single Bubble Memory Drive Capability
- Controlled-current Sinks Assure Proper Currents Independent of Variations in Bubble Gate Resistances
- Currents Independently Set by External Precision Resistors
- Temperature Compensation of Currents Via External Thermistor if Desired
- GENERATE Pulse Specially Shaped to Prevent Multiple Bubble Generation
- Pulse Time-out Circuit Protects Against Physical Damage in the Event of a Stuck Input Timing Signal
- On-chip High-voltage Source — System Interlocked until Proper Voltage is Present
- Chip Select Input for Multiple-bubble Systems
- Full Map Loop Read and Write Operation

PIN ASSIGNMENTS



28-pin Dual In-line
Package: 0.6-inch row spacing

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Value	Unit
Storage Temperature	−65 to +150	°C
Ambient Temperature with power applied Commercial Device Extended-temperature Device	 0 to +70 TBD to +85	 °C °C
Voltage — V_{BOOST}, IND, IREP, ISWAP	−0.2 to +35	Volts
Voltage — IGEN1, IGEN2, IMAP	−0.2 to +20	Volts
Voltage — V_{CC}	−0.2 to +7.0	Volts
Voltage — any other pin to GND	−0.2 to +6.0	Volts
Power dissipation	TBD	Watts

*Absolute Maximum Ratings indicate limits beyond which permanent damage may occur to the device. Proper operation of the device requires that it be limited to the conditions specified under DC Electrical Characteristics.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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PIN DESCRIPTIONS

Inputs

CS — Chip Select — enables the Operation Driver.

D_{IN1}, D_{IN2} — Data inputs (two channels).

$\overline{SYNC}$ — Data input clock (rising edge).

GEN — Trigger for GENERATE current pulses.

SWAP — Enable SWAP current pulse.

REP — Enable REPLICATE current pulse.

RMAP — Enable MAP-REPLICATE current pulse.

CUT — Timing for CUT portion of REPLICATE and MAP-REPLICATE current pulses.

Outputs

IGEN1, IGEN2 — GENERATE current pulses (two channels).

ISWAP — SWAP current pulse.

IREP — REPLICATE current pulse.

IMAP — MAP-REPLICATE current pulse.

$\overline{PDNO}$ — Power Down Output — indicates that V_{BOOST} is below its minimum operating value.

Supplies and Miscellaneous

GSET — GENERATE current set.

SWSET — SWAP current set.

TOSET — REPLICATE-TRANSFER current set.

RCSET — REPLICATE-CUT current set (adds to TRANSFER current).

V_{CC}(2) — Power supply voltage (2 pins).

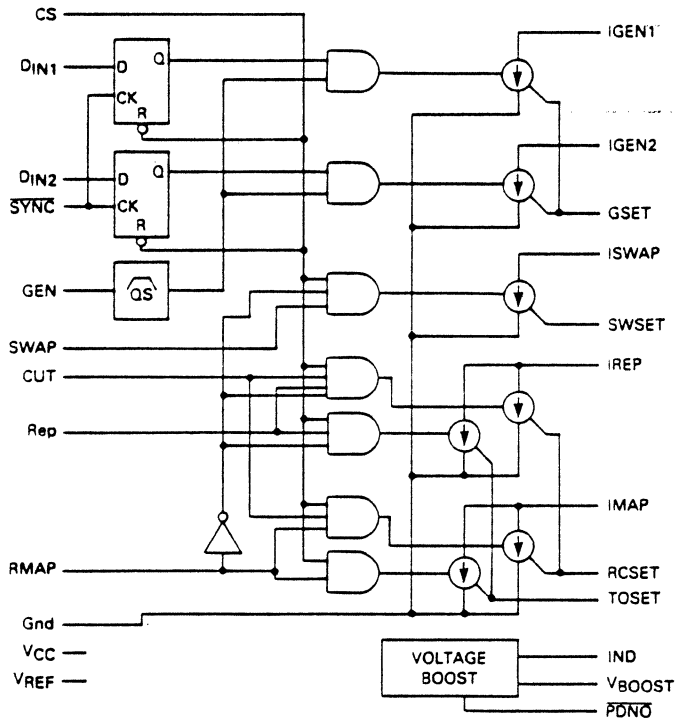
V_{REF} — Reference voltage used to set currents.

V_{BOOST} — High-voltage power supply output.

IND — Inductor and diode used in voltage-boost circuit (see application diagram).

GND(4) — System Ground (4 pins).

FIGURE 1 — FUNCTIONAL DIAGRAM



DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{REF} = 2.50 V ± 1%)

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.75	5.25	Volts
Power Supply Current	I_{CC}	—	100	mA
Current from V_{REF} (V_{REF} = 2.475 V)	I_{REF}	—	2.0	mA
Boost Supply Voltage	V_{BOOST}	28	35	Volts
Logic High In Voltage	V_{IH}	2.0	—	Volts
Logic Low In Voltage	V_{IL}	—	0.8	Volts
Logic Low Out Voltage (I_O = 4.0 mA)	V_{OL}	—	0.4	Volts
Logic High In Current (V_I = 2.7 V)	I_{IH}	—	10	μA
Logic Low In Current (V_I = 0.4 V)	I_{IL}	—	−1.6	mA
Output Leakage Current (Output Off)	I_{OL}	—	100	μA
IREP, ISWAP Saturation	V_{SATH}	—	6.0	Volts
Saturation Voltage — Other Outs	V_{SATL}	—	3.0	Volts

Note: The Bubble Memory Controller WRITE MAP command should not be executed more often than once per second, or the Operation Driver maximum power dissipation limit will be exceeded.

MC34046S ONLY (V_{REF} = 2.50 V ± 1%, Current Set Resistors = 6.04 kΩ ± 1% each)

Characteristic	Symbol	Min	Max	Unit
Generate Current	I_G	180	220	mA
SWAP Current	I_{SW}	25	31	mA
REPL-Transfer Current	I_{RT}	28	42	mA
REPL-Cut Current (Note 1)	I_{RC}	75	95	mA
MAP-REP-Transfer Current	I_{MT}	28	42	mA
MAP-REP-CUT Current (Note 1)	I_{MC}	75	95	mA

MC34047S ONLY (V_{REF} = 2.50 V ± 1%, Current Set Resistors = 6.19 kΩ ± 1% each)

Generate Current	I_G	190	230	mA
SWAP Current	I_{SW}	16	20	mA
REPL-Transfer Current	I_{RT}	30	40	mA
REPL-CUT Current (Note 1)	I_{RC}	130	150	mA
MAP-REP-Transfer Current	I_{MT}	16	20	mA
MAP-REP-CUT Current (Note 1)	I_{MCI}	65	75	mA

Note 1: CUT current is the sum of the currents determined by the resistors connected to TOSET and RCSET.

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit
DIN Setup Time	t_{DSU}	50	—	ns
DIN Hold Time	t_{DH}	50	—	ns
CUT Current Risetime (MC34047S only)	t_{CR}	—	50	ns
Other Out Current Rise	t_r	—	100	ns
IGEN Current Fall	t_{GF}	200	400	ns
CUT Current Falltime (MC34047S only)	t_{CF}	—	100	ns
Other Out Current Fall	t_F	—	200	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Unit
IGEN Pulse Width	t_{GW}	50	200	ns
CS to any Output	t_{CSO}	—	250	ns
GEN to IGENx Delay	t_{GGO}	—	200	ns
SWAP to ISWAP Delay	t_{SSO}	—	160	ns
Other In-Out Delays	t_{IO}	—	100	ns
SWAP Time-out	t_{STO}	—	80	μS
REPL-Transfer Time-out	t_{TTO}	—	50	μS
REPL-CUT Time-out	t_{CTO}	—	4.0	μS
GEN to SYNC	t_{GS}	1.1	—	μS

OPERATION

The magnetic bubble memory device requires a series of current pulses of proper timing, amplitude, and shape to generate and route the bubbles. These pulses are produced by the Operation Driver in response to signals generated by the controller.

The generate pulse creates a bubble in the input track. It is a fixed-width pulse triggered by the rising edge of the GEN input. A controlled fall time prevents multiple-bubble generation which can occur if the trailing edge is too sharp. Two generate outputs, IGEN1 and IGEN2, can drive separate bubble devices. They are independently enabled by data signals received on DIN1 and DIN2 respectively. The DIN signals are latched internally on the rising edge of $\overline{SYNC}$ prior to the GEN input. A high level on DINx will enable IGENx.

The Swap Pulse, ISWAP, causes an exchange of bubbles between the input track and the storage-loop tracks. It is on when the SWAP input is high. ISWAP is normally connected to the data swap gate on the bubble device, but if map loop write capability is required, it may be connected via a switch, jumpers, etc. to the map gate.

The replicate function copies bubbles from the storage-loop tracks onto the output track. A two-step pulse is used. A high-current, narrow initial portion cuts the elongated bubble in two; a lower-current, wider trailing portion transfers the trailing bubble onto the output track. Separate outputs are provided for data replicate, IREP, and map replicate, IMAP. These outputs are controlled by three input signals: REP or RMAP when high enables IREP or IMAP respectively; CUT when high enables the high-current portion of whichever pulse is simultaneously enabled.

The current levels of the various pulses are set by means of precision resistors connected externally between each of four pins and ground:

- GSET controls IGEN1 and IGEN2.
- SWSET controls ISWAP.
- TOSET controls the lower (transfer) level of IREP and IMAP.
- RCSET controls the initial (cut) portion of IREP and IMAP. This current is added to that determined by TOSET.

Temperature compensation of the currents for extended-temperature operation, can be done by using thermistor networks on the SET pins.

The Chip Select (CS) input is active high. When it is false (low) all current outputs are disabled. Since some of the current pulse levels, if sustained would damage the bubble device or the driver, a time-out circuit is included which will shut off any pulse if the input signal should remain active too long.

The higher resistance of the swap and data replicate gates requires a higher drive voltage than the normal power supply, V_{DD}. This voltage, V_{BOOST}, is provided by an on-chip voltage booster in conjunction with an external inductor, capacitor, and diode. When V_{BOOST} is below its specified range the Power Down Output signal $\overline{PDNO}$ is held low. This is an open-collector output signal and may be externally wire-ored.

FIGURE 2 — SIGNAL WAVEFORMS

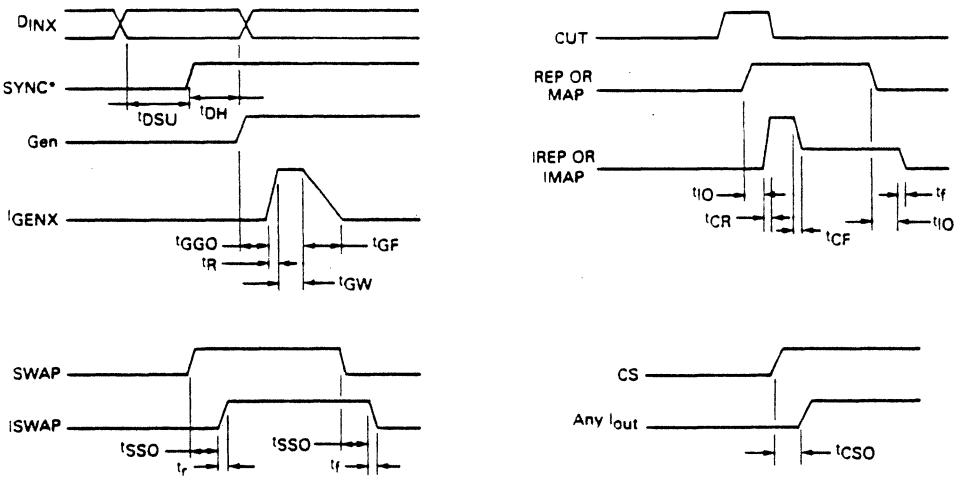
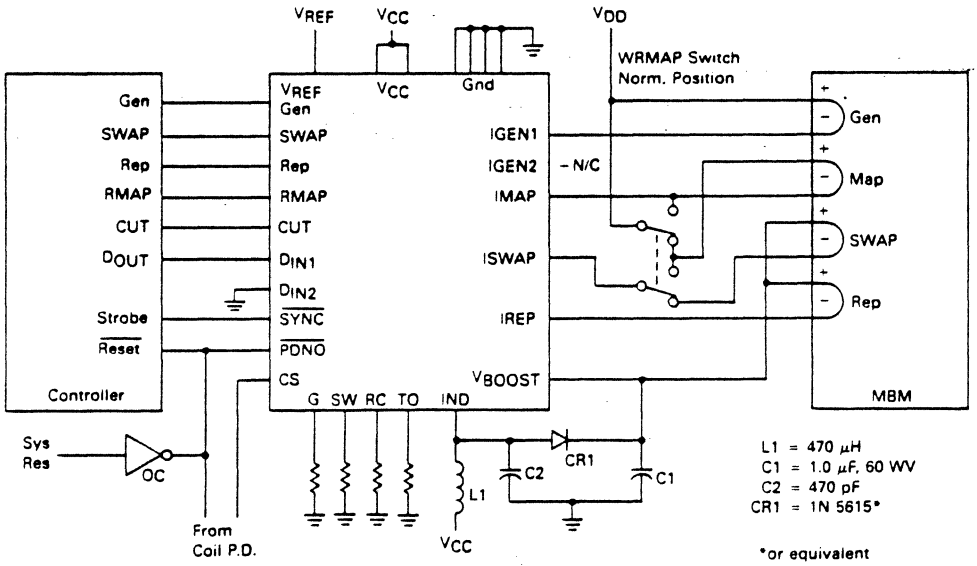


FIGURE 3 — TYPICAL APPLICATION OPERATION DRIVER



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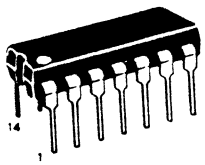
BUBBLE MEMORY PRODUCTS

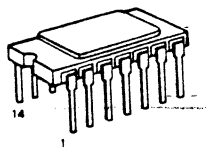
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MC34044

Advance Information

BUBBLE MEMORY SENSE AMPLIFIER





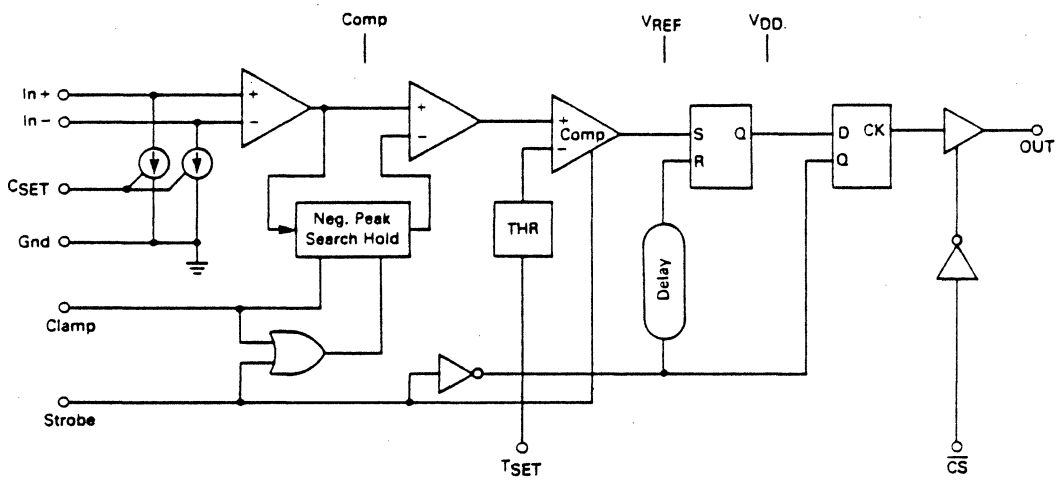
GENERAL DESCRIPTION

The MC34044 Bubble Memory Sense Amplifier is a monolithic bipolar linear integrated circuit which amplifies and detects the differential output signal of a magnetic bubble memory device. Peak-to-peak sensing is performed within a selected time window, thus rejecting noise which occurs outside that window. The Sense Amplifier circuit includes two matched, programmable current sinks which provide constant-current detector operation. The Sense threshold is externally selectable. The MC34044 is packaged in a 14-pin dual in-line package.

FEATURES

- True Peak-to-Peak Sensing
- Independent Time Windows for Negative and Positive Peak Detection Permit Rejection of Unwanted Signal Noise
- Constant Current Detector Operation — Currents Set by External Precision Resistor
- One of Three Preset Threshold Levels Selectable by User
- Linear Threshold Control from External Source Optional
- Noise Compensation Capacitor Reduces Susceptibility to Power Supply Noise
- Chip Select Input and Three-State Output for Multiple-Bubble Systems

FIGURE 1 — BUBBLE MEMORY SENSE AMPLIFIER FUNCTIONAL DIAGRAM



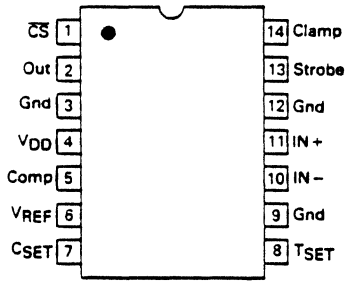
This document contains information on a new product. Specifications and information herein are subject to change without notice.

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ADI-774

PIN ASSIGNMENT

14-pin Dual In-line Package: 0.3-inch row spacing
also 14-lead Flat-Pack



PIN DESCRIPTIONS

Output (three-state)

OUT — Data Output — following the trailing edge of STROBE, indicates the state of the detected signal during the STROBE — high if the signal exceeded the threshold, low otherwise. Held in high-impedance state when $\overline{CS}$ is high.

Supplies and Miscellaneous

V_{DD} — Power supply voltage.

V_{REF} — Reference voltage for bias current and threshold.

GND(3) — System ground (three pins).

CSET — Detector current set resistor.

TSET — Threshold select.

COMP — Noise compensation capacitor.

Inputs

$\overline{CS}$ — Chip Select — enables the three-state data output.

IN+ / IN− — Differential sense signal input — negative peak detect and threshold are with respect to the indicated polarities. Also provides the detector bias currents.

CLAMP — Enables negative peak detection and activates peak hold function.

STROBE — Enables threshold comparator for positive peak detection. Trailing edge resets peak-hold function and enables OUT signal change.

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Value	Unit
Storage Temperature	−65 to +150	°C
Ambient temperature with power applied Commercial Device Extended-temperature Device	 0 to +70 −55 to +125	 °C °C
Voltage — V_{DD}, IN+, IN− to GND	−0.2 to +20	Volts
Voltage — any other pin to GND	−0.2 to +6.0	Volts
Power dissipation	TBD	Watts

*Absolute Maximum Ratings indicate limits beyond which permanent damage may occur to the device. Proper operation of the device requires that it be limited to the conditions specified under DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{REF} = 2.50 V ±1%)

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{DD}	10.8	18	Volts
Power Supply Current (Excludes I_D)	I_{DD}	—	25	mA
Current from V_{REF} (V_{REF} = 2.525 V)	I_{REF}	—	$0.1I_D + 0.2$	mA
Logic High In Voltage	V_{IH}	2.0	—	Volts
Logic Low In Voltage	V_{IL}	—	0.8	Volts
Logic High Out Voltage (I_O = −4.0 mA)	V_{OH}	2.7	—	Volts
Logic Low Out Voltage (I_O = 1.6 mA)	V_{OL}	—	0.4	Volts
Logic High In Current (V_I = 2.7 V)	I_{IH}	—	20	μA

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{REF} = 2.50 V ±1%)

Parameter	Symbol	Min	Max	Unit
Logic Low In Current (V_I = 0.4 V)	I_{IL}	—	−1.6	mA
Output Off-State Current (V_O = 0.4 − 2.7 V)	I_{OZ}	−20	20	μA
Detector Current	I_D	$10*V_{REF}/R_{SET}$ ±10%		
Detector Current Mismatch	I_{DM}	—	2%	—
IN+, IN− DC Voltage	V_{ICR}	3.0	V_S − 3.0	Volts
Differential DC IN Volts	V_{IND}	—	200	mV
AC Common-Mode IN Volts	V_{ICM}	—	200	mV
Low Threshold Voltage (V_{TSET} = V_{REF})	V_{TL}	TBD	TBD	mV
Nominal Threshold Voltage (TSET pin open)	V_{TN}	TBD	TBD	mV
High Threshold Voltage (V_{TSET} = 0.0 V)	V_{TH}	TBD	TBD	mV

Note 1: Includes 1% tolerance on R_{SET}.

AC ELECTRICAL CHARACTERISTIC (T_A = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit
$\overline{CS}$ to OUT	t_{CO}	—	300	ns
$\overline{CS}$ to OUT Disable	t_{CZ}	—	300	ns
STROBE to OUT Change	t_{SO}	—	300	ns
Delay Differential IN to Comparator Output	t_d	—	300	ns

OPERATION

Detection of a magnetic bubble within the memory device utilizes the magnetoresistive effect whereby a bubble passing beneath the detector element causes a change in its resistance. By passing a constant current through the detector, this resistance change can be sensed as a voltage change. A matched reference element which is not in the path of the bubble permits the use of differential sensing to cancel noise introduced by the rotating field.

The Sense Amplifier circuit contains matched constant-current sinks for the active and reference detector elements. These elements should be connected beween the supply voltage and the IN+ and IN− pins respectively. These pins are connected internally to the current sinks. The current levels are matched and are set by meeans of a precision resistor connected externally between the CSET pin and ground. A thermistor may be used to provide a temperature-compensated detector current if required for extended-temperature operation of the magnetic bubble memory.

A differential amplifier across the two detector elements amplifies the bubble signal. The difference signal is fed to a negative peak detect-and-hold circuit, and to another difference amplifier. The difference between the signal and the negative peak is fed to a voltage comparator where it is compared to a threshold voltage. A signal which exceeds the threshold indicates the passage of a bubble beneath the detector. One of three predetermined threshold voltages can be selected by connecting the TSET pin to V_{REF} or to GND or leaving it open. For extended-temperature operation, linear control of the threshold can be accomplished by applying a linear voltage to TSET.

Timing is provided through the CLAMP and STROBE inputs. CLAMP enables the negative-peak detector. The most-negative voltage appearing while CLAMP is high is stored until the trailing edge of STROBE. The output of the threshold comparator is enabled while STROBE is high. if the signal exceeds the negative peak by the threshold amount at any time while STROBE is high, a ONE is detected and latched. The output pin changes state at the trailing edge of STROBE. CLAMP and STROBE may be connected together and driven with a single signal.

The COMP pin may be used to reduce the effect of power supply noise on the detector. A capacitor connected between COMP and V_{DD} increased the supply rejection performance of the internal regulator with respect to noise present on V_{DD}. The best value will depend upon the individual system, and is typically 0.1 μF.

The Chip Select ($\overline{CS}$) input is active-low. When $\overline{CS}$ is false (high) the three-state data output (OUT) is placed in the high-impedance state. Several Sense Amplifiers may have their OUT pins connected together with only one circuit enabled at a time via the $\overline{CS}$ pin.

FIGURE 2 — SIGNAL WAVEFORMS

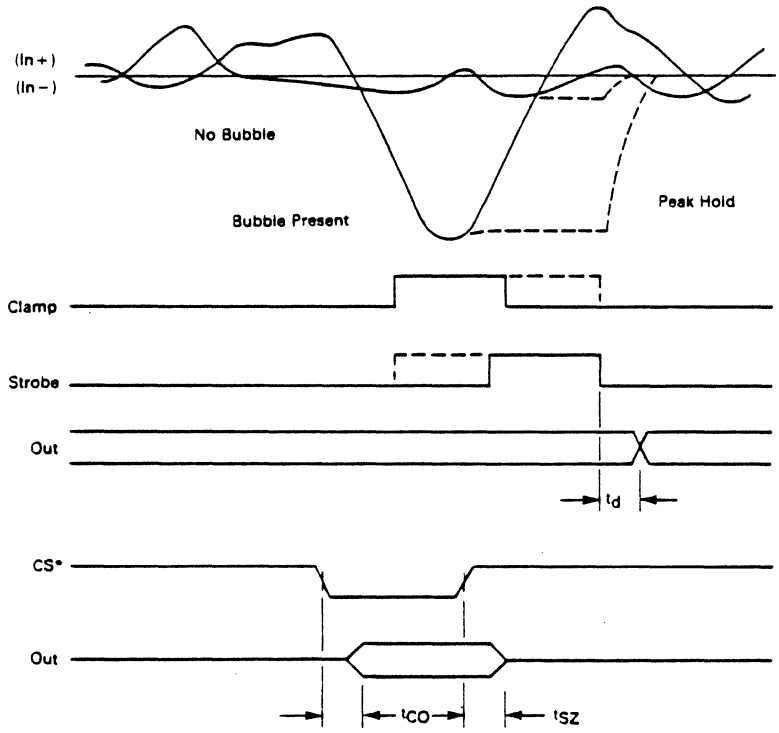
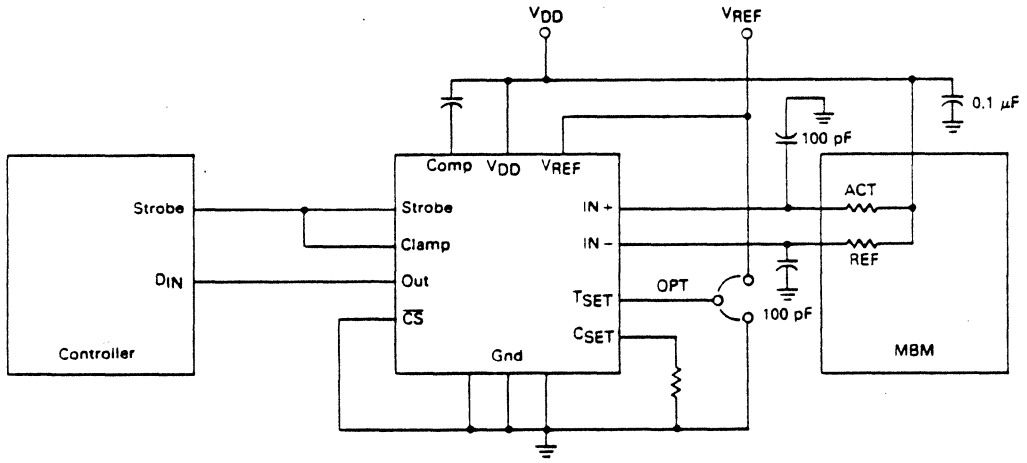


FIGURE 3 — TYPICAL APPLICATION



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BIOGRAPHICAL SKETCH

Richard John Brzozowy was born in Milwaukee, Wisconsin, on December 8, 1957. He received his elementary education in a Milwaukee parochial school and secondary education at the Milwaukee Trade and Technical High School. In 1976, he entered the Milwaukee School of Engineering, graduating in 1980 with a Bachelor of Science degree in Electrical Engineering. While still pursuing his undergraduate education, he worked briefly with disk storage systems for IBM - General Systems Division in Rochester, Minnesota. In May 1980, he joined the Motorola Integrated Circuit Applications Research Laboratory (MICARL) in Mesa, Arizona as a system design engineer in the Bubble Memory Development area, where he has remained since. At Motorola, he is responsible for the design and development of the Motorola family of bubble memory system products.